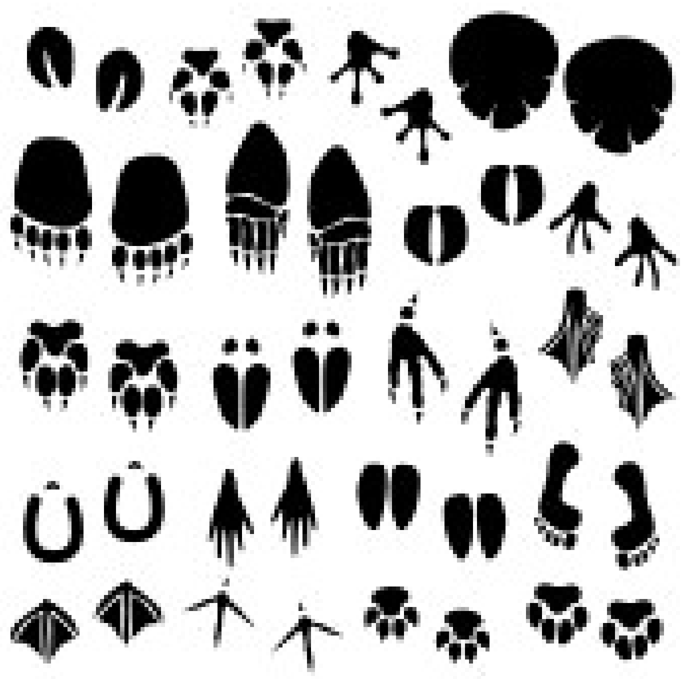
ASICS POUR LES DÉTECTEURS DE TRACES

eric.delagnes@cea.fr

Ecole IN2P3 de Microélectronique 24-27 juin 2013

ASICS pour les détecteurs de trace

- Introduction
- ASiCs pour les trajectographes Silicium
- ASICs pour les trajectographes gazeux
- Bibliography



- **Détection uniquement des traces de particules chargées => sinon détection indirecte,**

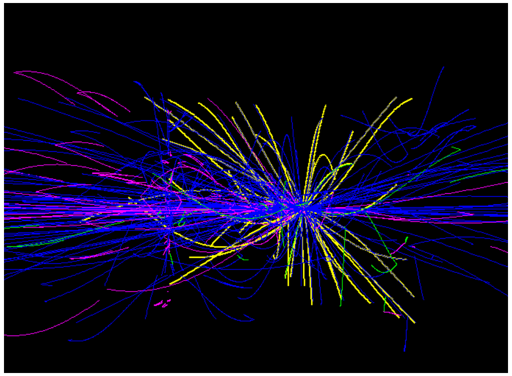
- Construction d’évènements,

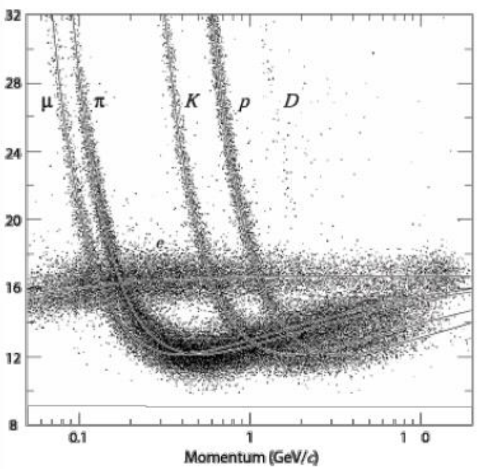
- Mesure de la courbure de traces dans un champs magnétique: spectromètre => mesure de l’impulsion et du signe de la charge,

- Identifier et déterminer la position des désintégrations de particules issues des interactions dans un collisionneur (vertexs secondaires),

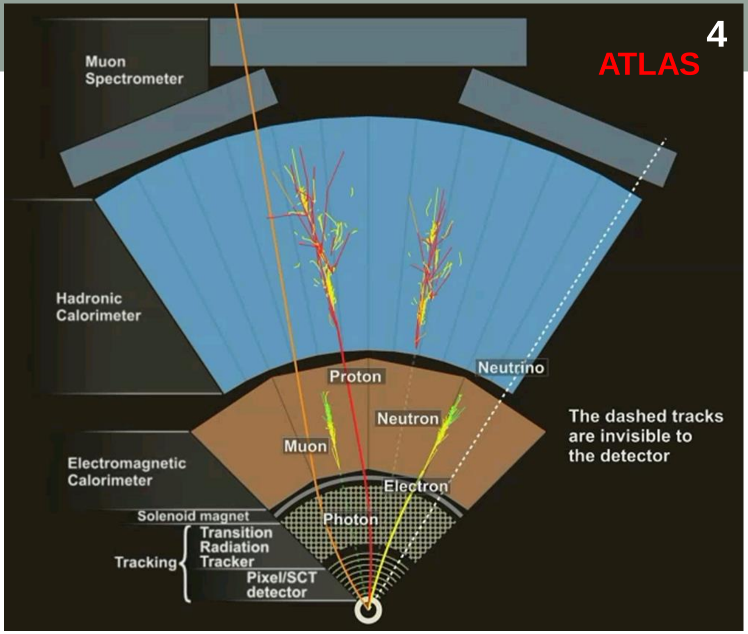
- Impulsion + dE/dx => Identification de particules,

- En Ph. Nucléaire : connaitre la cinématique des particules du faisceau avant leur interaction avec la cible

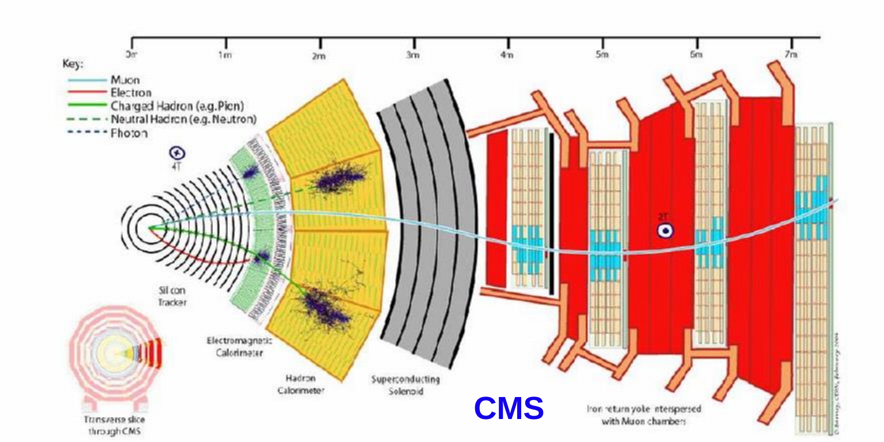




Types de détecteurs de Trace



- Plaque photographique, émulsion
- Gaz:
  - Compteur Geiger, chambre à fils,
  - MSGC, GEM, Micromegas,
  - TPC, TRT
- Liquide :
  - Chambre à bulles
- Solide :
  - Scintillateur
  - Silicium :
    - STRIPS
    - PIXELS
    - MAPS
    - DEPFET
    - CCD



Principe Général:

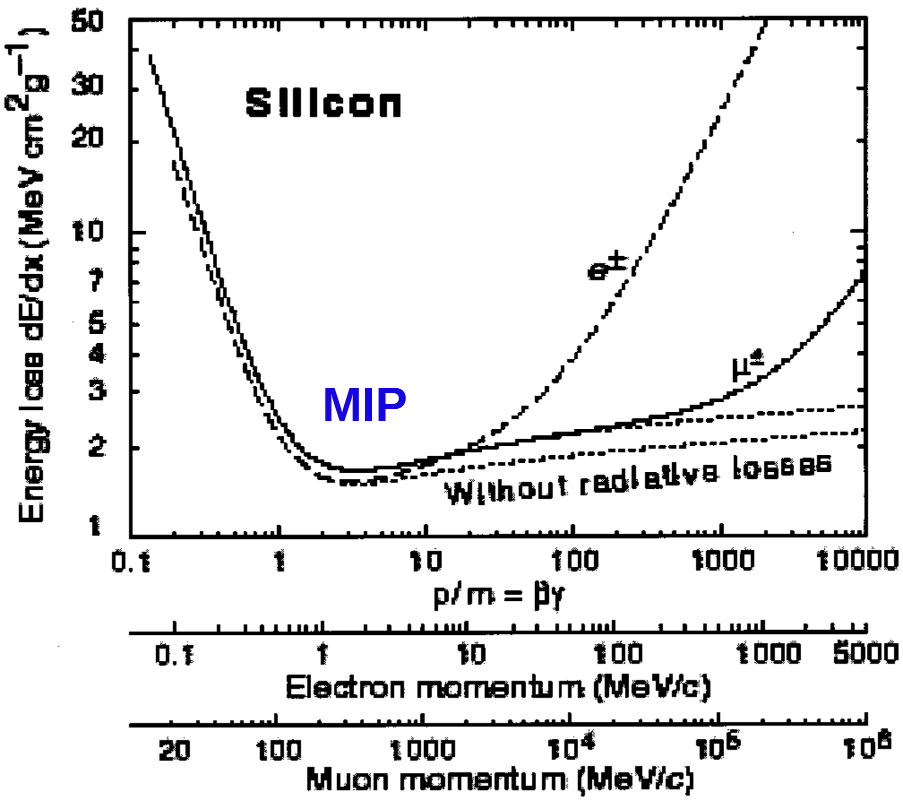
- Ionisation du milieu,
- Détection du passage d'une particule chargée en mesurant la charge totale (e-+ions) produite par l'ionisation du milieu.
- La détection doit perturber le moins possible le trajet de la particule(<> calorimètre) : diffusion multiple, X0,

Detectors for Tracking : Typical rate / response time.

Type	Response Time	Rate
EMULSION	Static	static
BUBBLE CHAMBER	s	Hz
WIRE CHAMBER	µs	10kHz
TPC	µs	10kHz
Si MAPS	>100 ns	
MPGD	20-100 ns	MHz
Si DETECTOR	10 ns	10 MHz
SCINTILLATOR + PM	ns	> MHz
MCPPMT	100 ps	MHz

Mean Linear enrgy deposition : Bethe-Bloch formula

$$\frac{dE}{dx} = -2\pi N Z \frac{z^2 e^4}{m\beta^2}\left(\ln \frac{2m\gamma^2\beta^2 E_{cut}}{I^2} - \frac{\beta^2}{2}\left(1 + \frac{E_{cut}}{\Delta E_{max}}\right) - \frac{\delta}{2}\right)$$



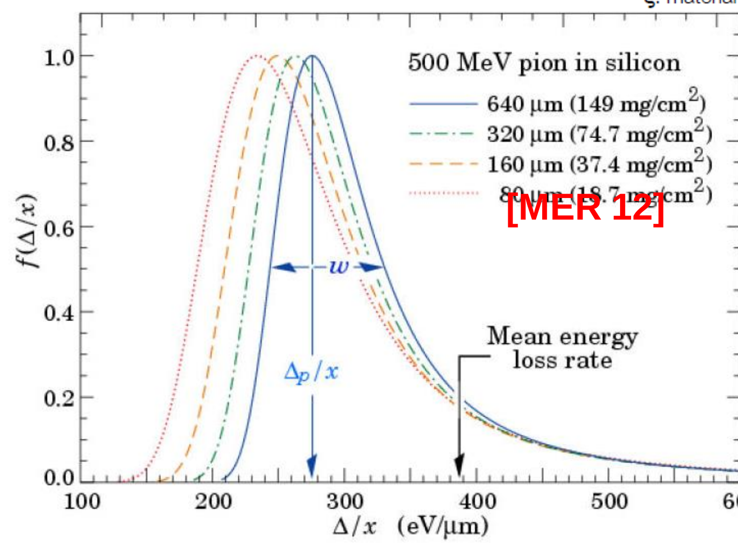
For detector thins/ particle range: Large statistics fluctuations of energy loss in ionisation

⇒ Landau distribution:

Approximation:

$$f(\Delta/x) = \frac{1}{\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{\Delta/x - a(\Delta/x)_{\mathrm{mip}}}{\xi}\right) + e^{-\left(\frac{\Delta/x - a(\Delta/x)_{\mathrm{mip}}}{\xi}\right)}\right]$$

ξ: material constant



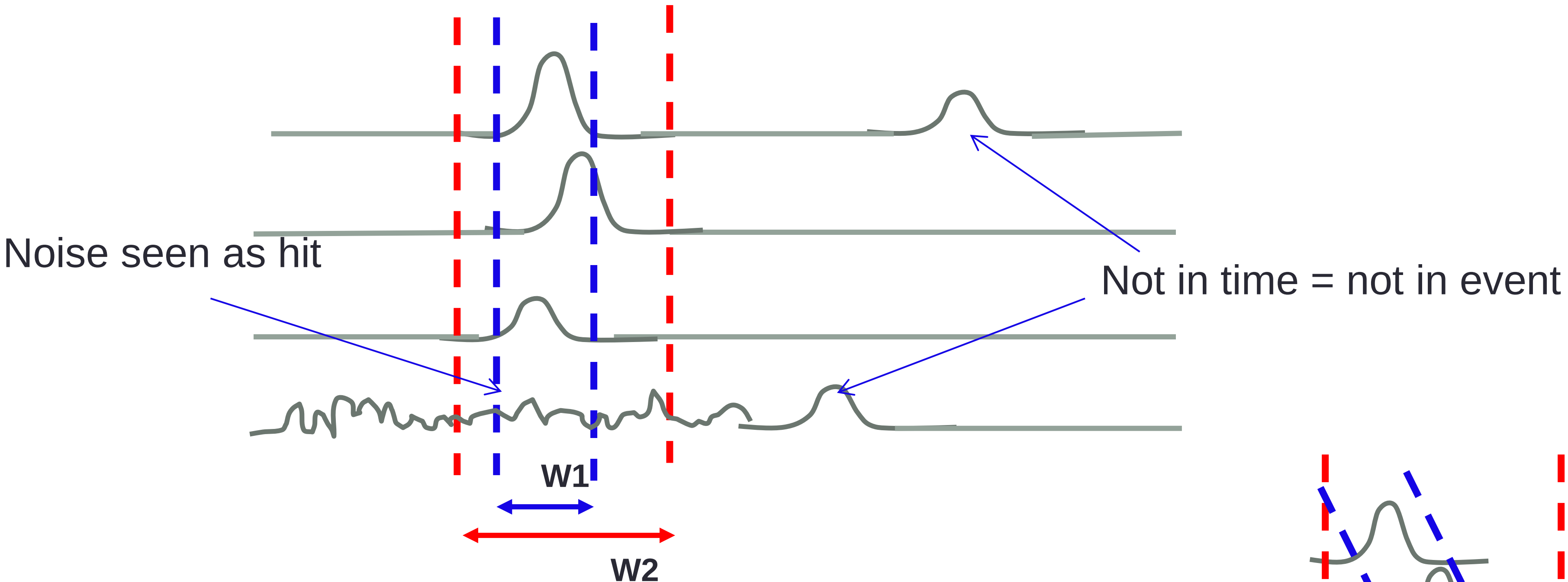
Asymetic: very difficult to measure mean value

⇒ Most probable value

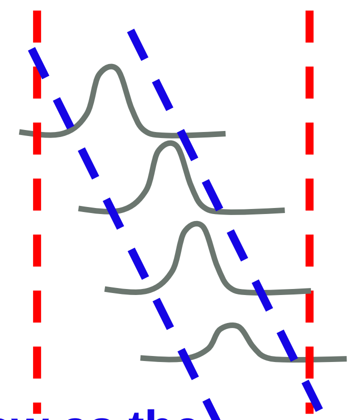
Thinner = more spread

- **Serie of events within a time window**

- **Higher rate or high background/noise => Smaller time window.**



- **Fix window defined by a Trigger or**
- **Sliding window in the case of TPC or Silicon Drift**
- **May have several levels of acceptance time window**



- **For colider, it is convenient (but not nessary) to define the window as the bunch crossing period**
- **Track Topology => remove noise: track is an object, not a collection of points**

- **High Threshold to avoid false noise hit.**

For a Noise with Gaussian amplitude distribution, the noise frequency depends on filtering (f0), noise and threshold (Rice equation):

$$f_{noise} = \frac{f_0}{2} e^{-\frac{V_{th}^2}{2\sigma^2}}$$

shaping

Not true if Pickup !!!

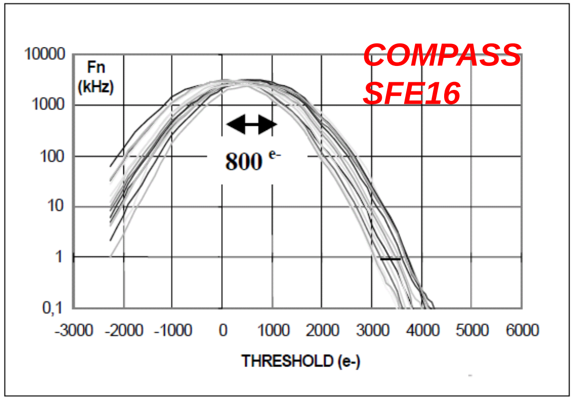
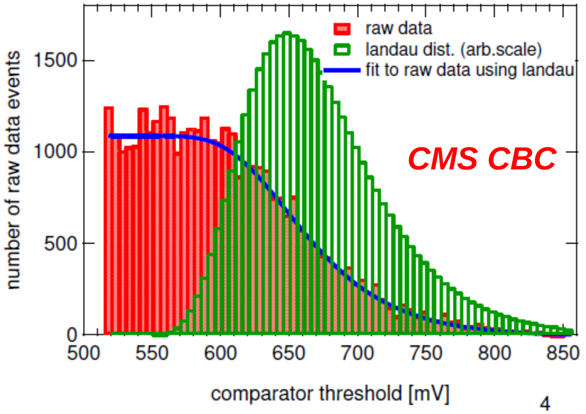
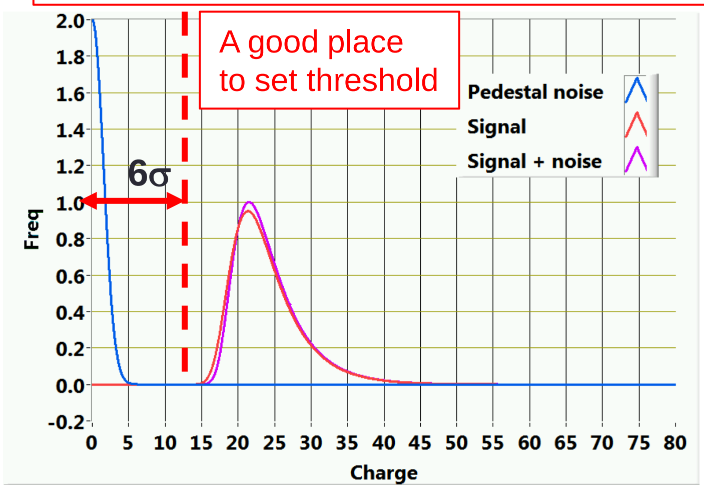


Figure 9 : Frequency of Noise hits versus threshold value (16 channels of a typical chip). The input capacitance is 32pF.

- **Low Threshold to have a good efficiency :**

$$Eff = Detector\ Efficiency \times \int_{Vth}^{\infty} Q\, dQ$$





Threshold spread and noise on threshold must be taken into account « noisy channels) to set the threshold

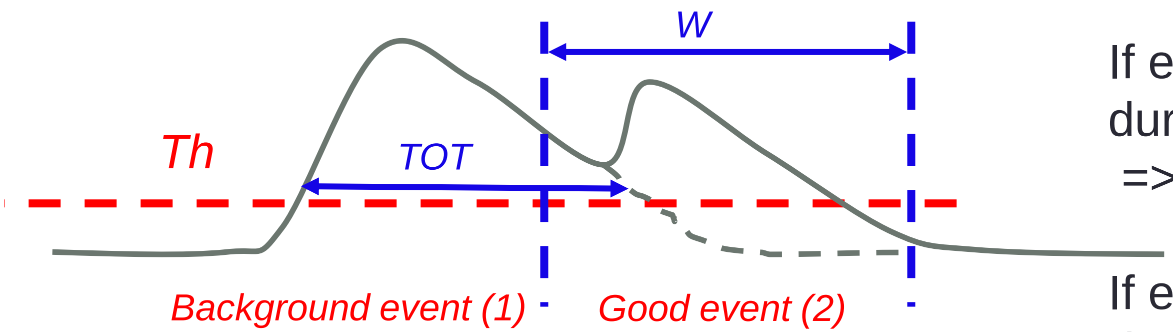
A noisy channel can « kill » the acquisition

Occupancy

- **Hit can also be missed because the electronics is doing something else:**

$$Occ.Ineffiency = rate\ (incl.Background) \times \frac{TOT}{Window}$$

Time over Threshold
Signal width



If event defined by Th Xing during W:
=> Event 2 missed.

If event defined by amplitude > Th during W:
=> Event 1 considered as good

- Other strategies possible if waveform known
- Symetric shaping better for occupancy
- Tracking IS timing

Shaping time = tradeoff between noise and occupancy
The best way to decrease occupancy is to segment the detector => pixel

Centroïd calculation (seeW. Dulinski 's lesson @ Frejus for exemple)

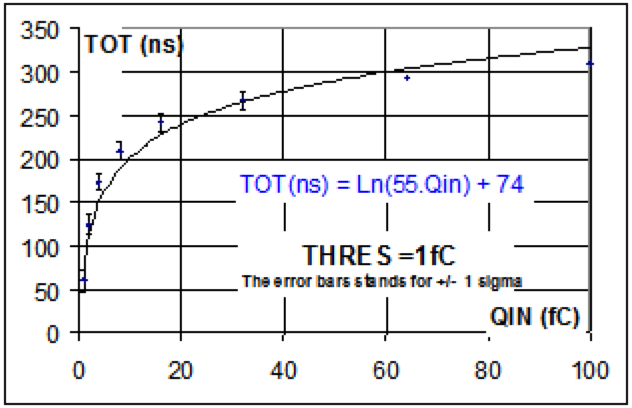
- If « binary » readout, position resolution is limited by quantification:

$$\sigma = \frac{Pitch}{\sqrt{12}}$$

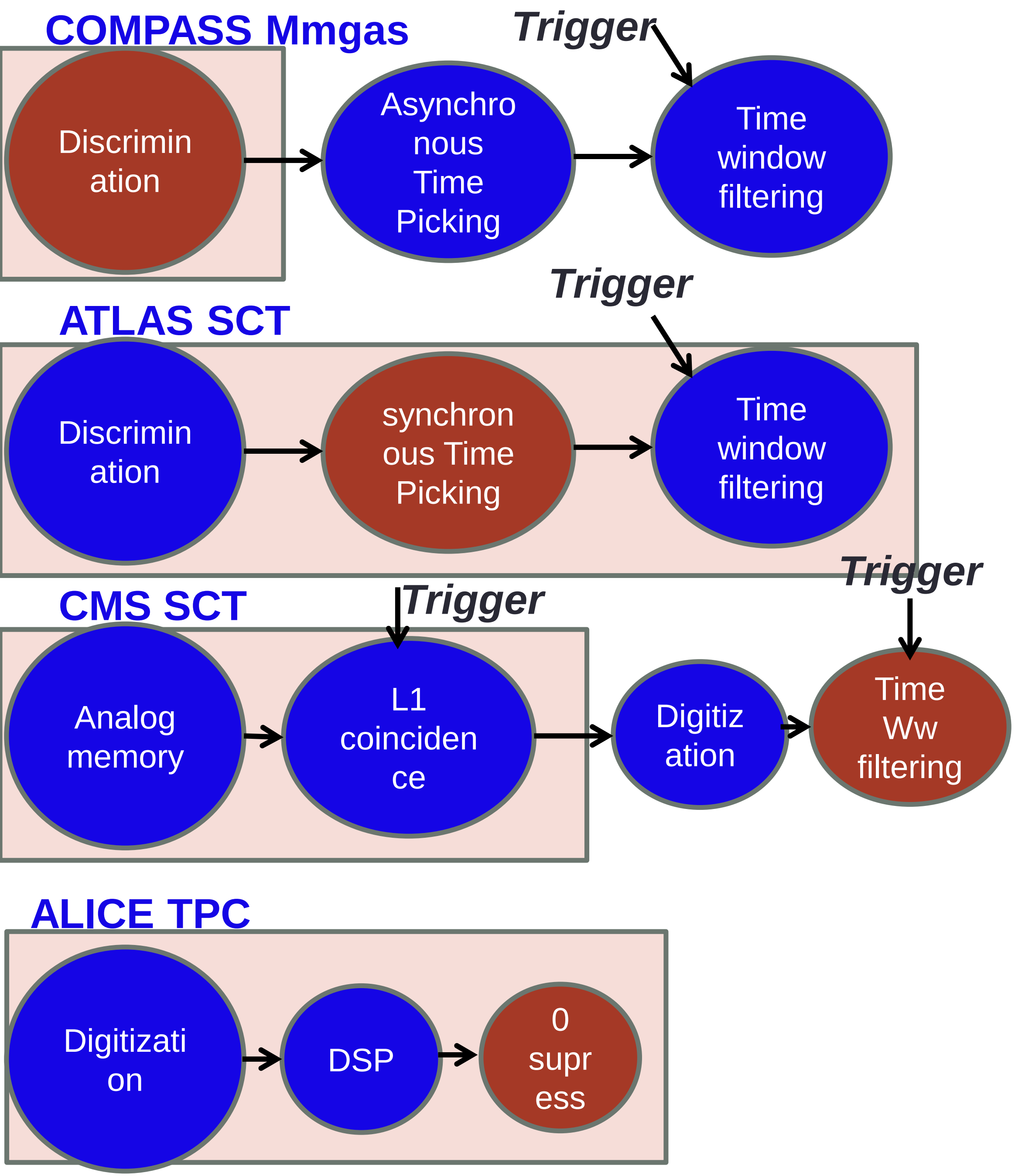
- In Gas or semiconductor detectors, Position resolution can be dramatically improved by centroïd calculation:
  - ⇒ Requires cluster size >2 => increase occupancy
  - ⇒ charge shared => less S/N, risk of non efficiency
  - ⇒ For large spread, position information is given by the tails of the charge deposition profile => dynamic range

  Good S/N required

  - ⇒ Analogue or pseudo-analogue readout => more complex readout
- Relation Charge/Time Over Threshold can be used to estimate the Charge for a small effort.



Possible architectures



- ☺ Low data volume
- ☺ Can participate to a trigger
- ☺ Simple, low power
- ☹ Decision taken early
- ☹ Sensitivity to noise (common mode noise)

- ☺ Low data volume
- ☺ Simple, low power
- ☹ Decision taken early
- ☹ Sensitivity to noise (common mode noise), less than previous

- ☺ Decision taken at the end
- ☺ Digital treatment possible
- ☹ Large volume of data
- ☹ Complexity

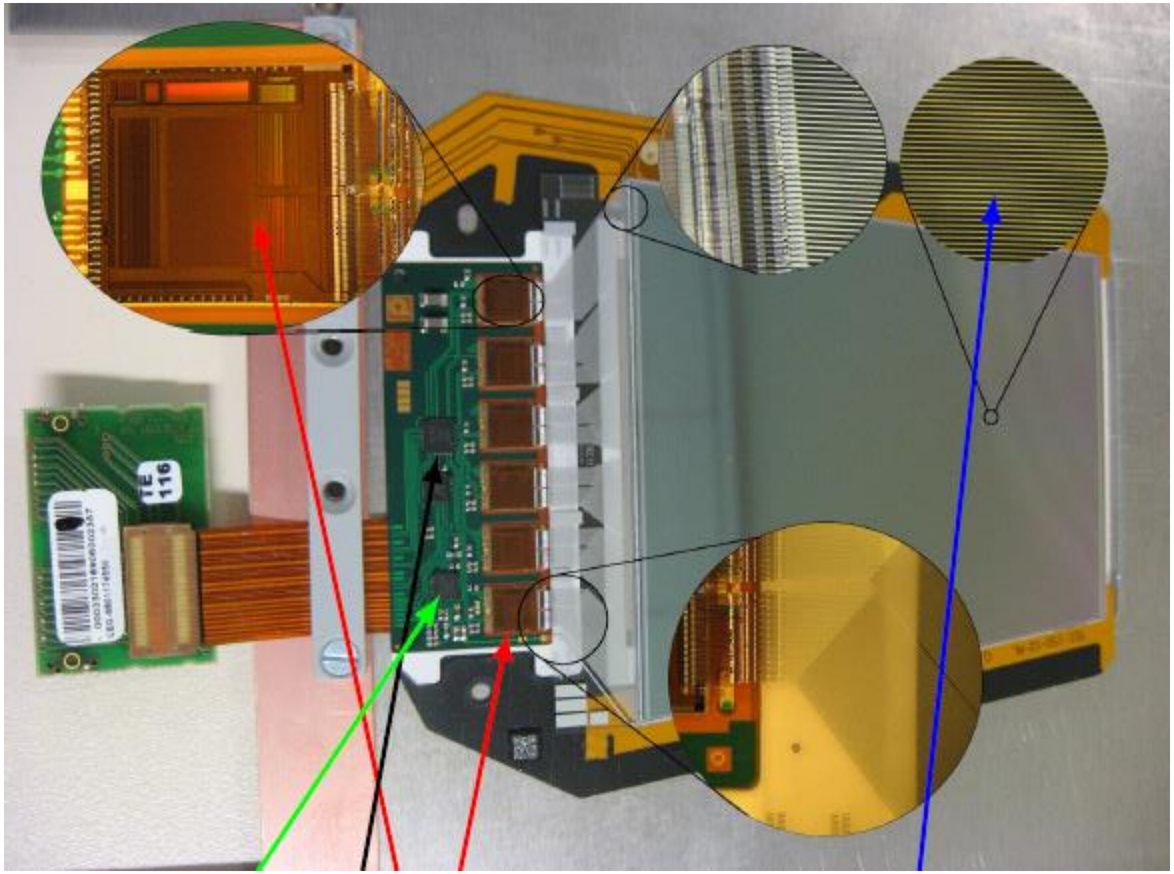
- ☺ Decision taken at the end
- ☺ Digital treatment possible
- ☹ Power consumption
- ☹ Area
- ☹ Complexity

Analog front-end circuits => see R. Hermel's lecture

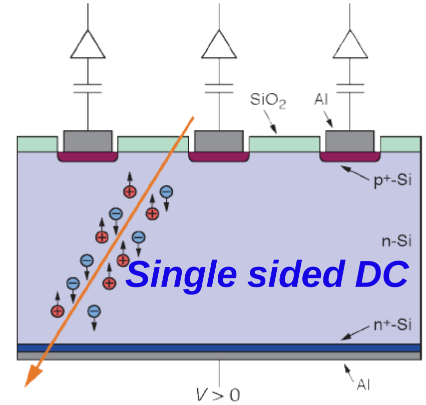
- **Front end amplifier design**
  - **Scaling and optimization**
    - Detector capacitance
    - Technology generation
    - Power and speed

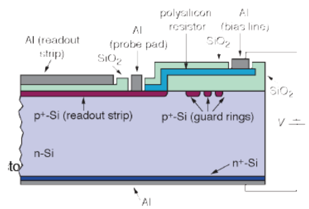
- **Signal processing**
  - **Continuous time filter, "RC" network**
    - Asynchronous
    - Issue: low noise passive reset
  - **Time variant filter, "switched capacitors"**
    - Synchronous timing
    - Issue: signal processing of random events with a simple readout scheme

Silicon Strip Detectors

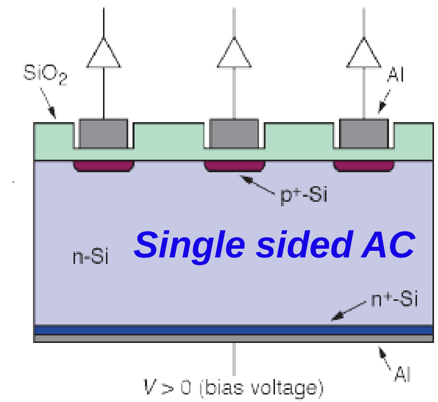


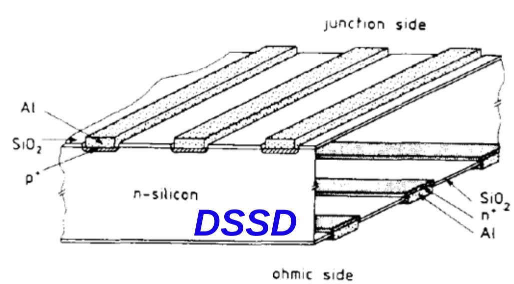
- **Solid-State Ionization chamber**
- **p-n junction reverse biased forms the detection zone**
- **Ionization along the track of the high-energy particle (e-h+) in the depletion region**
- **For 300µm Si detector the most probable signal for a Minimum Ionizing article is around 3.5fC (non-irradiated detector)**
- **Drift of the charge in the electric field**
- **Current induced by this drift collected by the FE electronics**
- **Spatial resolution provided by the segmentation of the detector**





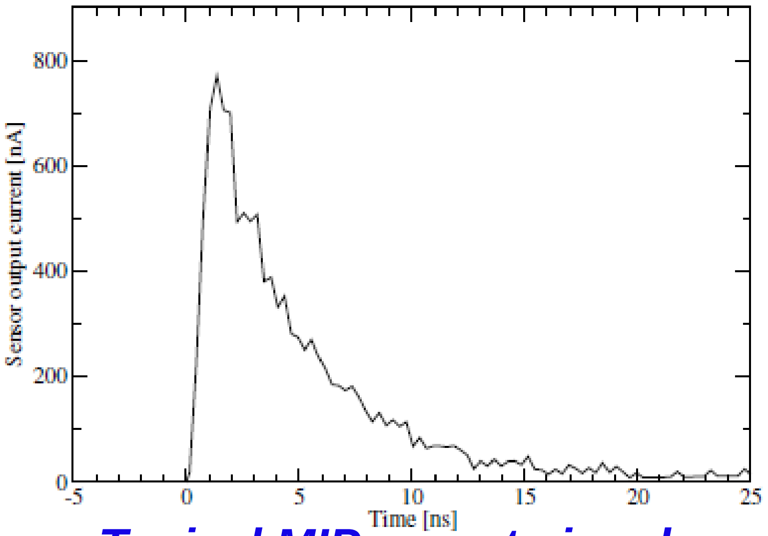
On detector bias resistors





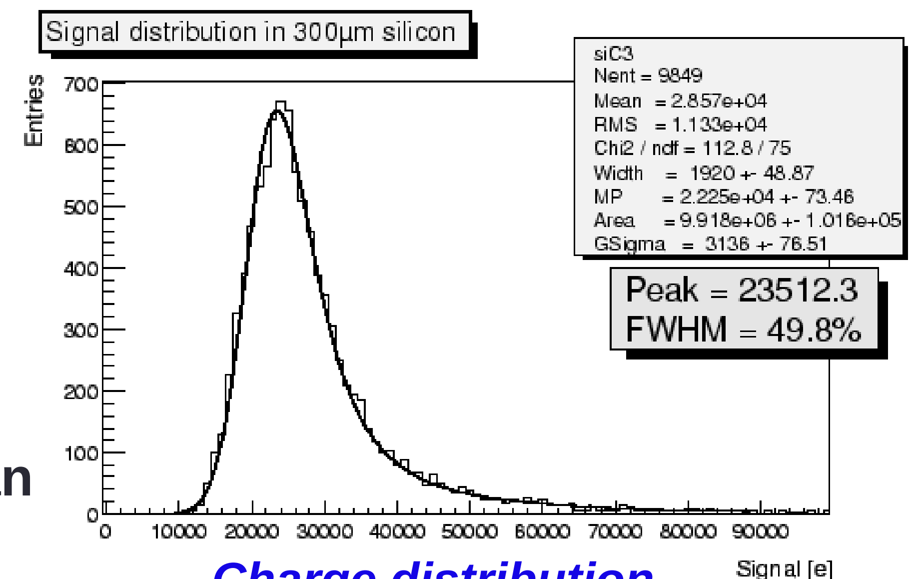
Silicon Detector signal (in a thin detector)

- **Duration dominated by hole drift**
- **Short duration < 15ns**



Typical MIP curent signal

- **Asymmetric Landau distribution**
- **No charge < 10000 e-**
  => very good efficiency
- **Long Tail**
- **Mean charge difficult to measure**
- **Most probable value easy**
- **Here: convoluted with the gaussian distribution of the noise**



Charge distribution

Les détecteurs Silicium: avant les ASICs

1960 Détecteurs Si

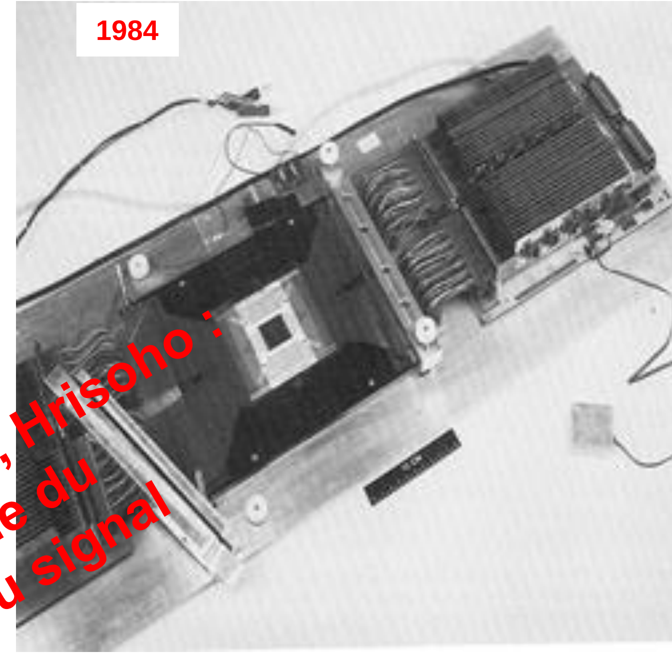
SEMICONDUCTOR DETECTOR SYSTEMS (dE/dx AND E) FOR THE DETECTION AND MASS IDENTIFICATION OF PROTONS, DEUTERONS, TRITONS, He^3 AND ALPHA PARTICLES IN THE 10 TO 30-MeV ENERGY REGION

H. E. WEGNER
LOS ALAMOS SCIENTIFIC LABORATORY, UNIVERSITY OF CALIFORNIA, LOS ALAMOS, NEW MEXICO
UNITED STATES OF AMERICA

Abstract — Résumé — Аннотация — Resumen

Semiconductor detector systems (dE/dx and E) for the detection and mass identification of protons, deuterons, tritons, He^3 and alpha particles in the 10 to 30-MeV energy region. In the 10 to 30-MeV region of energy many different reactions can occur in a charged-particle scattering experiment and, without proper mass identification, complex spectra from different reactions are superimposed and in many cases impossible to analyse. A semiconductor detector system

1984



Gatti, Manfredi, Radeka, Chase, Hrisoho : base theorique du traitement du signal

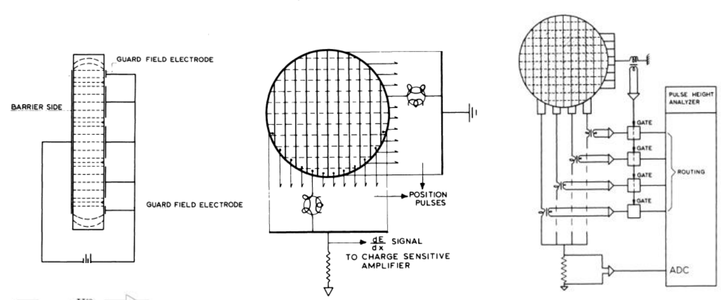
Détecteurs Si double face => XY

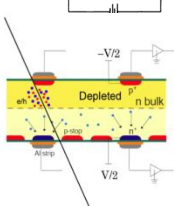
1966

IEEE TRANSACTIONS ON NUCLEAR SCIENCE June

THE CHECKER BOARD COUNTER: A SEMICONDUCTOR dE/dx DETECTOR WITH POSITION INDICATION

W. K. Hofker, D. P. Oosthoek, A. M. E. Hoeberechts
Philips Research Laboratories, N. V. Philips' Gloeilampenfabrieken
Eindhoven, The Netherlands





[Hof66]

Nuclear Instruments and Methods in Physics Research A243 (1986) 153–158
North-Holland, Amsterdam
SERVICE D'INFORMATION SCIENTIFIQUE 153

1985

FIRST RESULTS FROM A SILICON-STRIP DETECTOR WITH VLSI READOUT

Giuseppina ANZIVINO, Roland HORISBERGER, Leonardus HUBBELING and Bernard HYAMS
CERN, Geneva, Switzerland

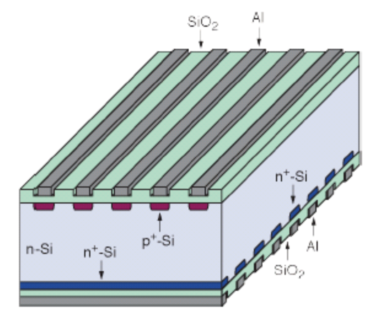
Sherwood PARKER and Alan BREAKSTONE
University of Hawaii, Honolulu, Hawaii, USA

Alan M. LITKE
University of California at Santa Cruz, Santa Cruz, California, USA

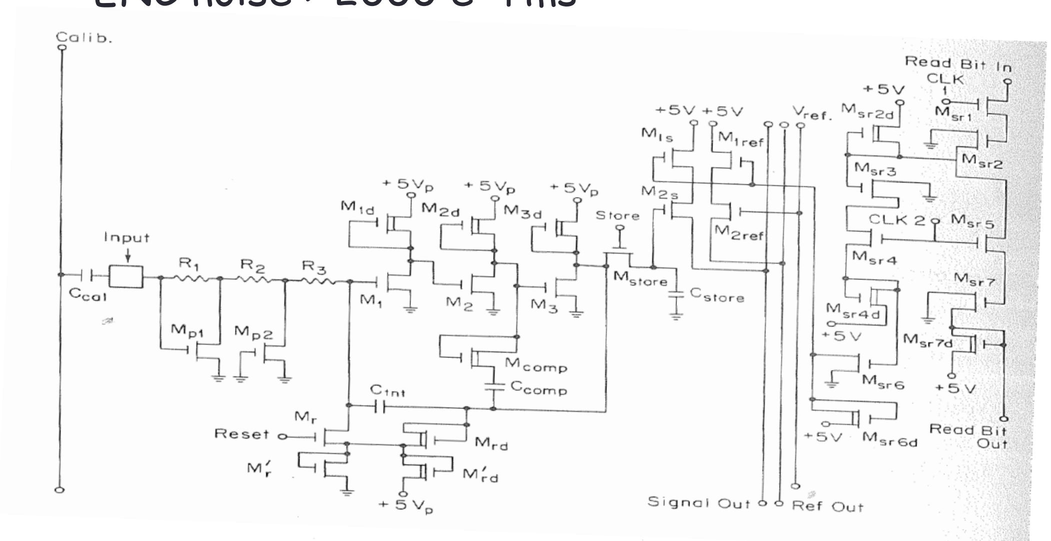
James T. WALKER
Stanford University, Stanford, California, USA

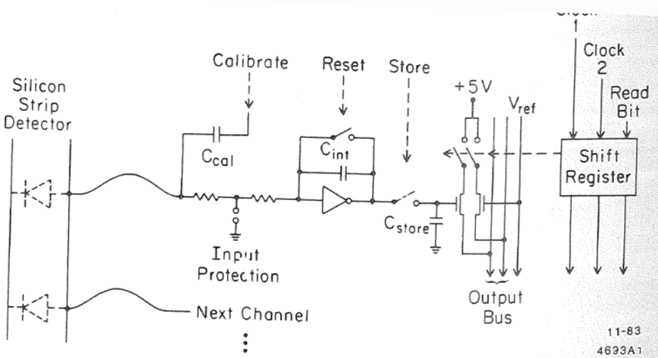
Nils BINGEFORS
University of Uppsala, Sweden

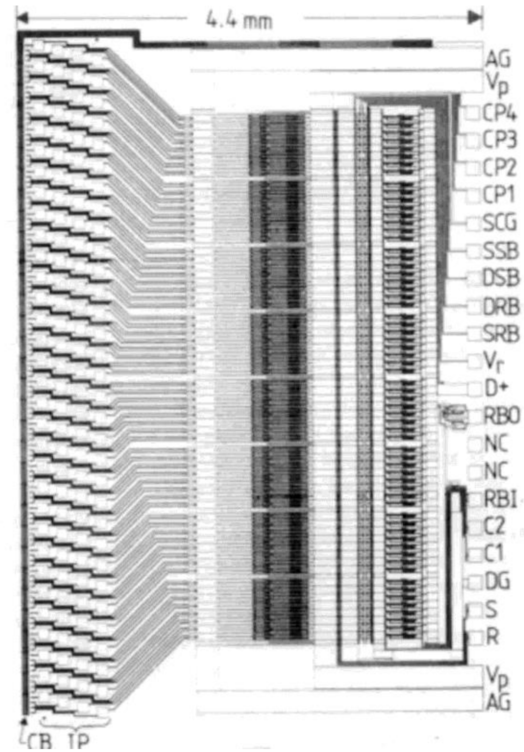
Received 6 August 1985



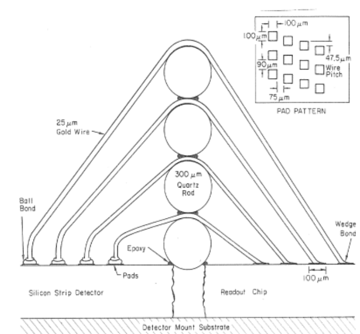
- ✓5μm NMOS technology
- ✓128 channels, 6.4x4.4 mm
- ✓Simple amplifier, no cascod, with T&H
- ✓No shaping
- ✓Mux Output
- ✓Power 1.6W
- ✓ENC noise > 2000 e- rms



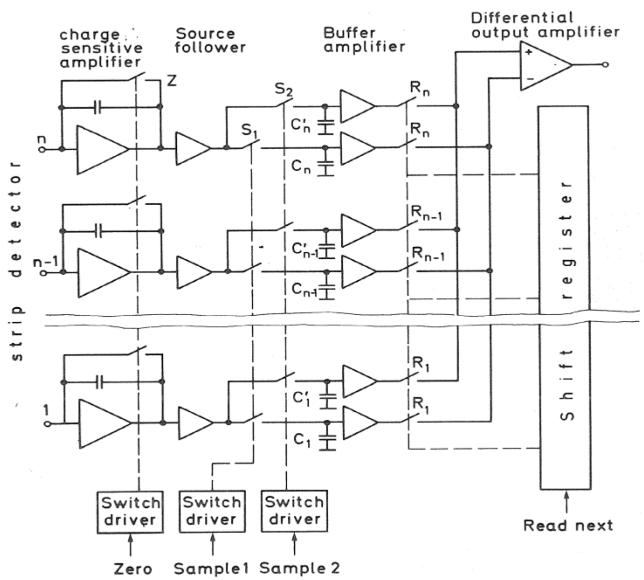




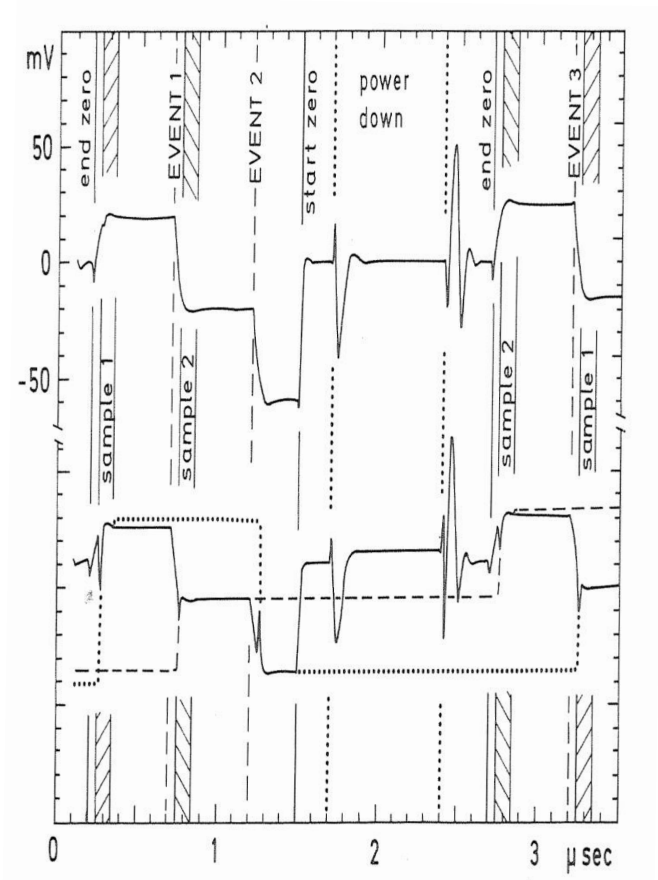
[Walk 84]



Dans le même numéro de NIM: R. Hoffman et G. Lutz (MPI)



✓CDS
✓Multiplexing



✓Power pulsing

CMOS technology has been chosen for the realization of the readout concept. The disadvantage of somewhat higher space use is offset by the many advantages possible:

– Single stage high gain amplifiers (gain above 1000) can be built. This alleviates the problems with unwanted oscillations.

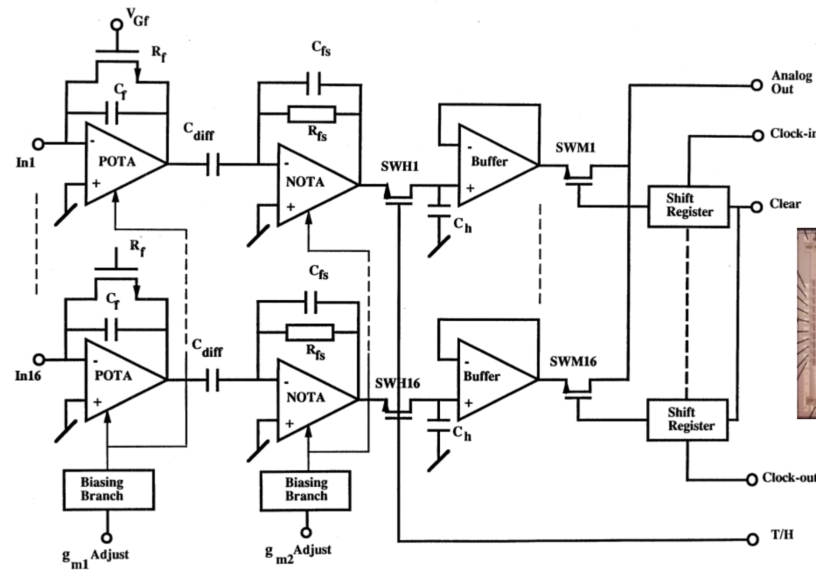
– Circuits can be realized which can be turned on and off very fast (~ 200 ns). This property can be used to reduce the average power consumption by turning down the electronics when it is not needed (e.g. outside beam spill).

– Making use of symmetries, circuits can be designed which are fairly insensitive to variations in technology parameters (e.g. threshold voltage) and hopefully also to

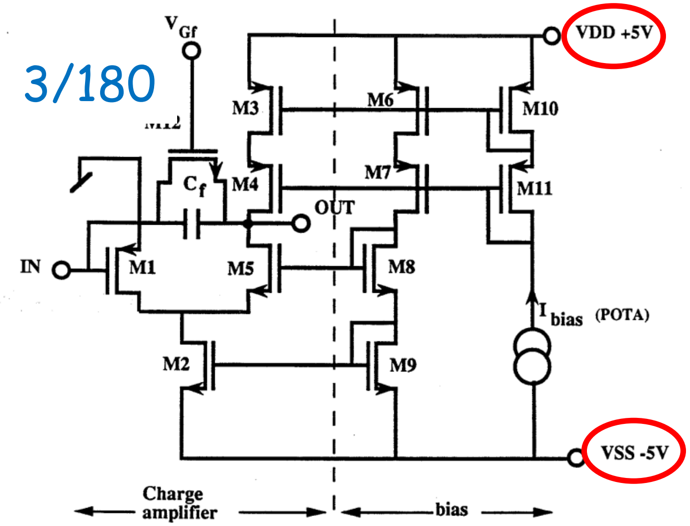
[Hof 84]

[BEU90],

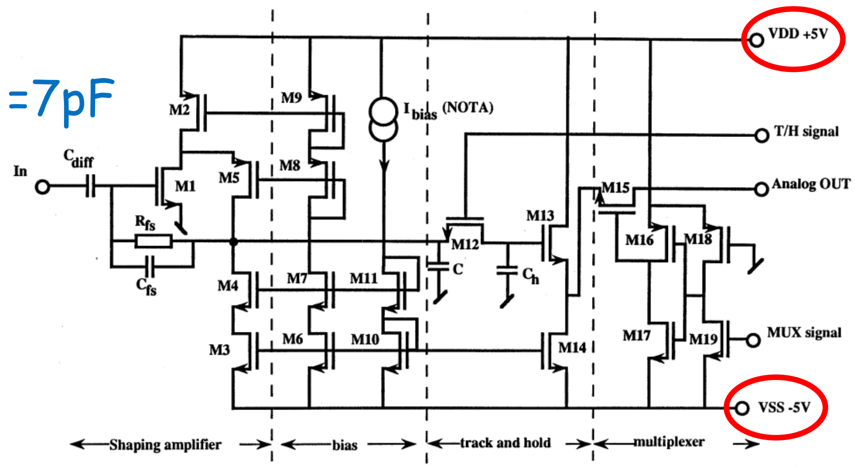
- ✓MIETEC 3µm CMOS technology
- ✓16 channels of Ampli-shaper
- ✓Mulitplexed output
- ✓5mV/fC
- ✓1.1mW/Ch
- ✓750 ns peaking time
- ✓1000 e- rms/ Cdet = 20 pF



3/180



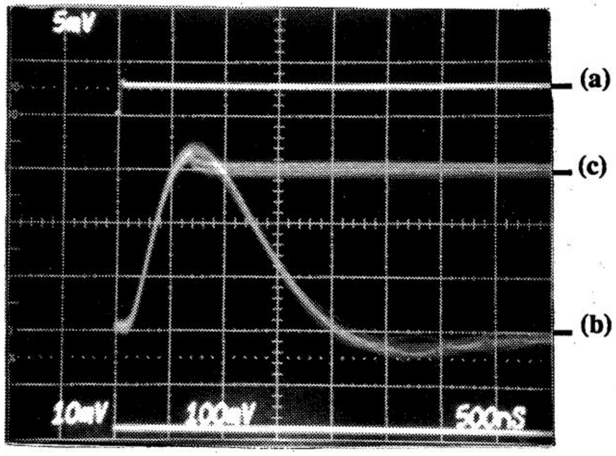
Cdif =7pF

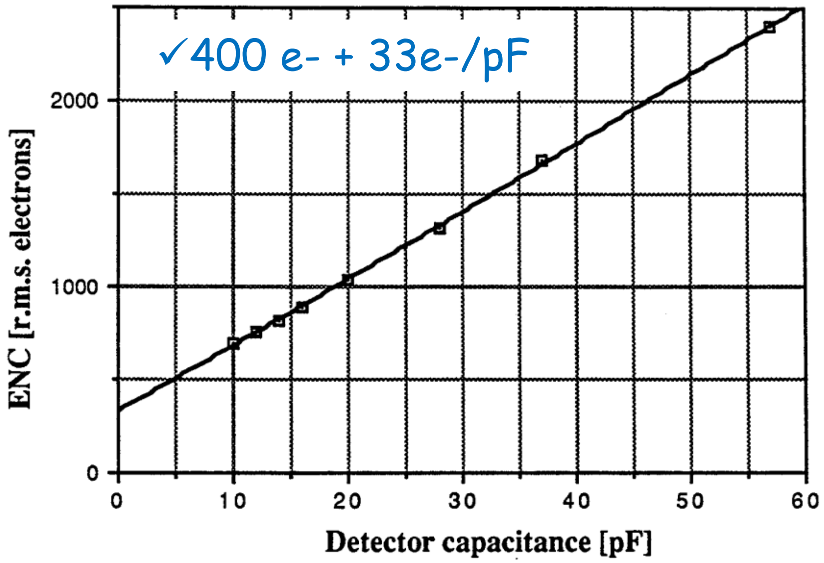


Continuous Reset: Long MOS
Folded Cascode configuration

Shaping = CSA pole + Rf_sCf_s
Cdif + $1/gm_{Sh}$
Tunable via bias currents

AMPLEX : use in UA2 inner tracker



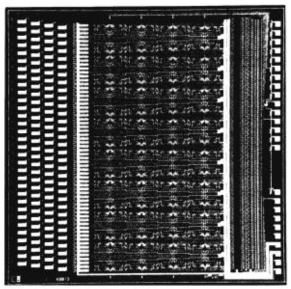


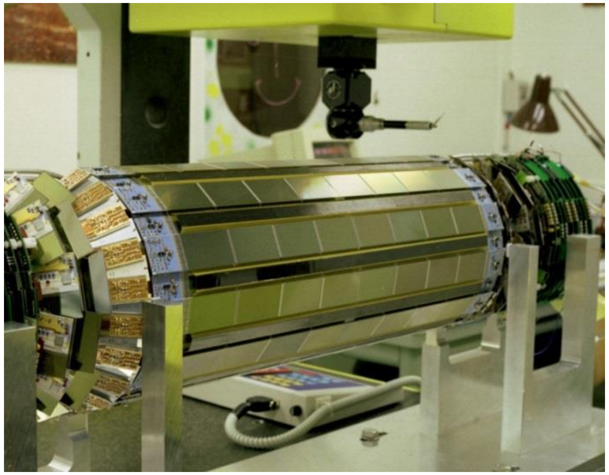
Tracking at LEP 14/07/1989-2/11/2000

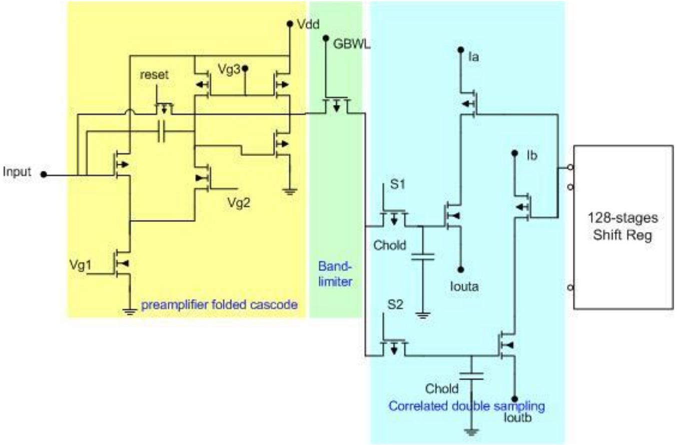
	ALEPH	DELPHI	L3	OPAL
Layers	2	3	2	2
Radii [cm]	6.3, 11.0	6.6, 9.2, 10.6	6.4, 7.9	6.1, 7.4
Modules/layer	9, 15	24, 20, 24	12	12, 15
Sensors/module	6	4, 8	4	5
Module length [cm]	40	28, 48	28	30
Max $\lvert\cos\theta\rvert$	0.88, 0.95	0.91, 0.93	0.83, 0.93	0.89, 0.93
Channels	95,000	150,000	73,000	65,000
Front-end chip	MX7-RH	MX6, TRIPLEX	SVX-H3	MX7, MX7-RH
Sensor-type	double-sided	double + single	double-sided	single-sided
Readout pitch [μm]				
ϕ	50	50	50	50
z	100	44 - 176	150, 200	100
Cooling	Water + Air	Water	Water	Water + Nitrogen
Sensitive area [m^2]	0.96	1.37 + 0.41(VFT)	0.52	0.53

✓All the LEP experiments used a Si tracker
✓Low multiplicity => Strip
✓Slow Shaping

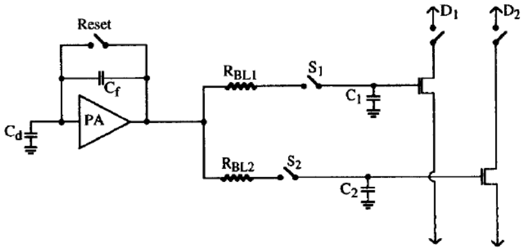
Inner layers
MX6 (RAL) [ARD 92], 128 ch, Evolution of MX3 chip
MIETEC 3μm CMOS. 7.1 mm x 6 mm
ENC=325 e-rms + 23 e/pF @ 1.8μs

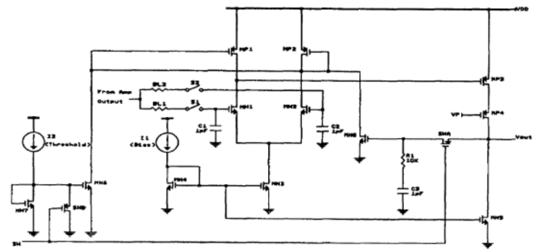




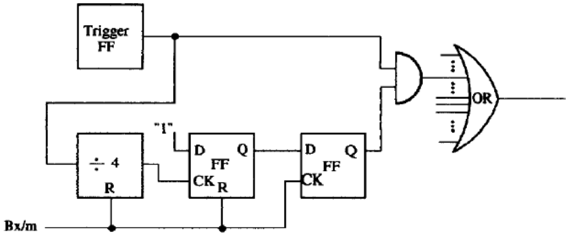


Outer layers:
Triplex (LAL) [ARD94],
AMS 1.2μm
128 ch, 55 mW
Protection resistors removed
Shaping time 0.5μs
ENC ~ 320 e-rms + 20 e/pF
Or for delphi trigger





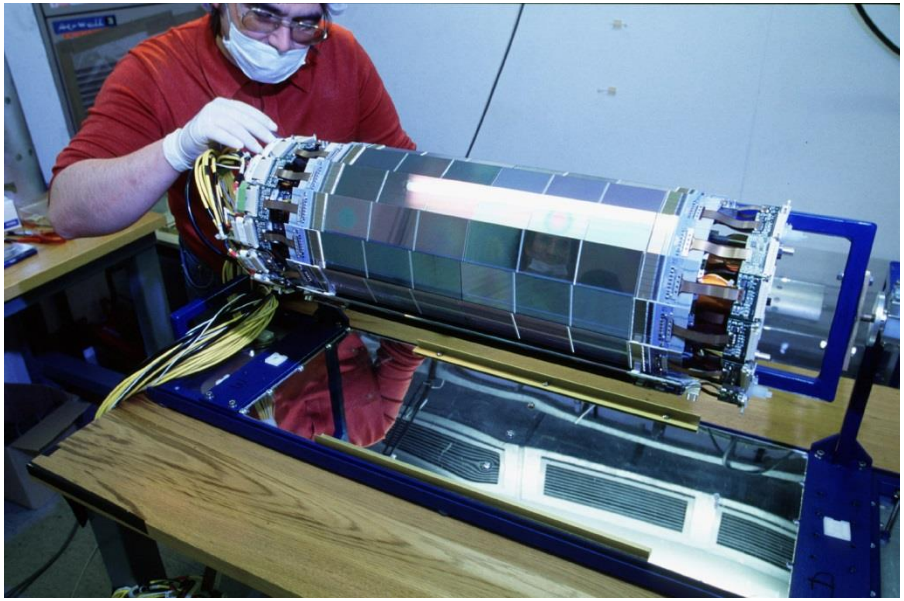
AUTO ZERO Comparator



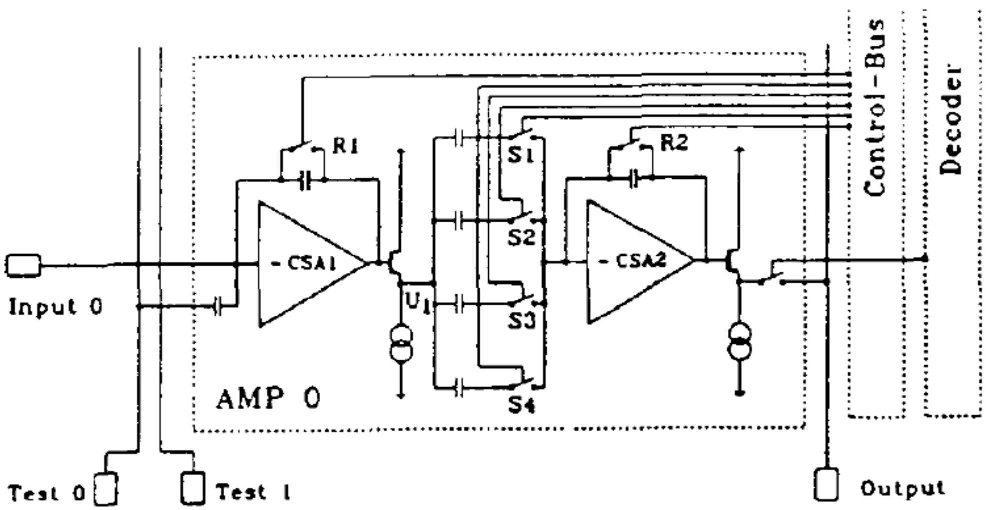
Or output with noisy channel disconnect

ALEPH Microvertex

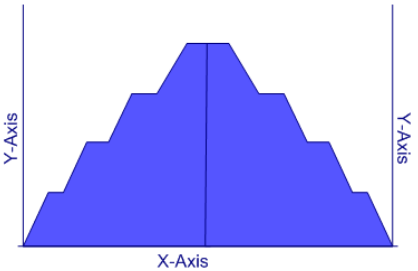
[BEC 89],



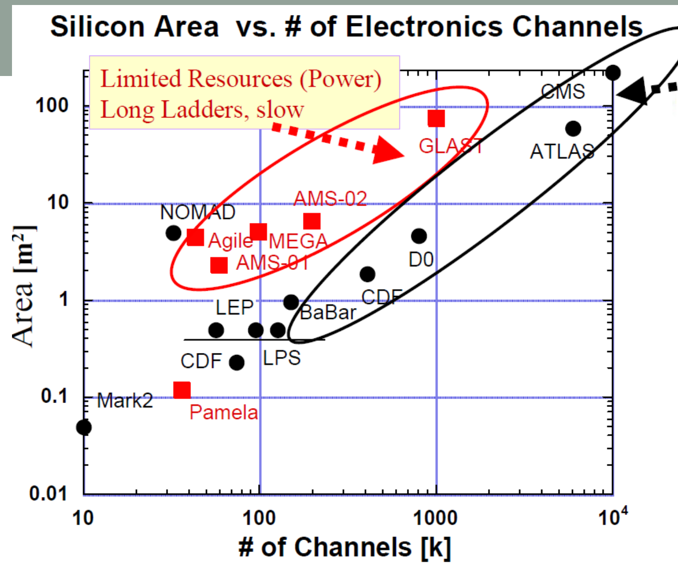
CAMEX (MPI)
- 64 channels, 6.35 x7.8 mm
- ENC=330 e- rms+ 30 e-/pF @ 1μs
- Gain=70mV/fC
- <2mW/ch adjustable
- Offset compensation, Ileak
- >15krad radtol



Multiple correlated sampling
- 4 samples before signal
- 4 samples after signal
- Weighting function close to ideal



From LEP to LHC (~ 2000s)



- Generalisation of hybrid pixels for the inner Detectors (not studied in this lecture) already introduced at the end of LEP (Delphi)
- New constraints for strip detectors

	LEP	LHC (1)
Power/channel	2 mW	1 mW
Timing capability for BX Id/ shaping	20µs ~1.5µs	25 ns 25 ns
Typical Strip Length	6 cm	10 cm
Trigger rate		100 kHz
Events / Bunch Crossing	1	10-100
Radiation Lvl	10s krads	>10 Mrads
Compactness	A lot of cables	Very high

Fast Shaping required

Serie noise now dominent
In LEP strong contibution of 1/f and //.

Practically S/N degraded only from 40 -> 15.

New trade-off noise/speed
New architectures.

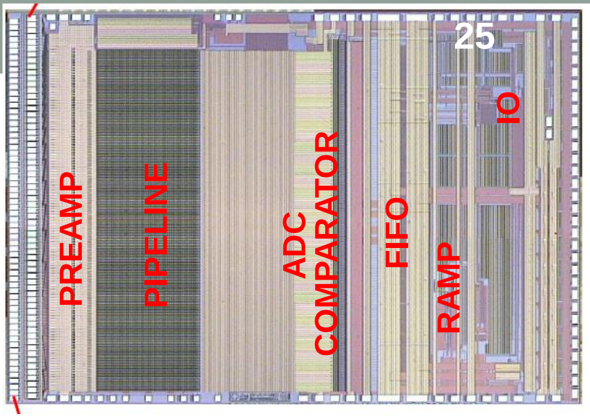
Slow control, readout,services inside the chips

Rad-Hard Designs
Detector damage

Buffering

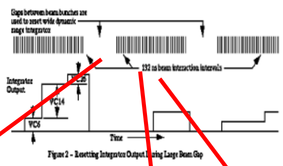
SVX chips for Tevatron's experiments [Kri04]

- Last member of the **SVX** family
- 128 Channels, **2mW**/channel. SlowControl for many param
- **On L1 request** , digitization of all channels.
- Use for both CDF and D0, run II
- 10-50pF strip detectors

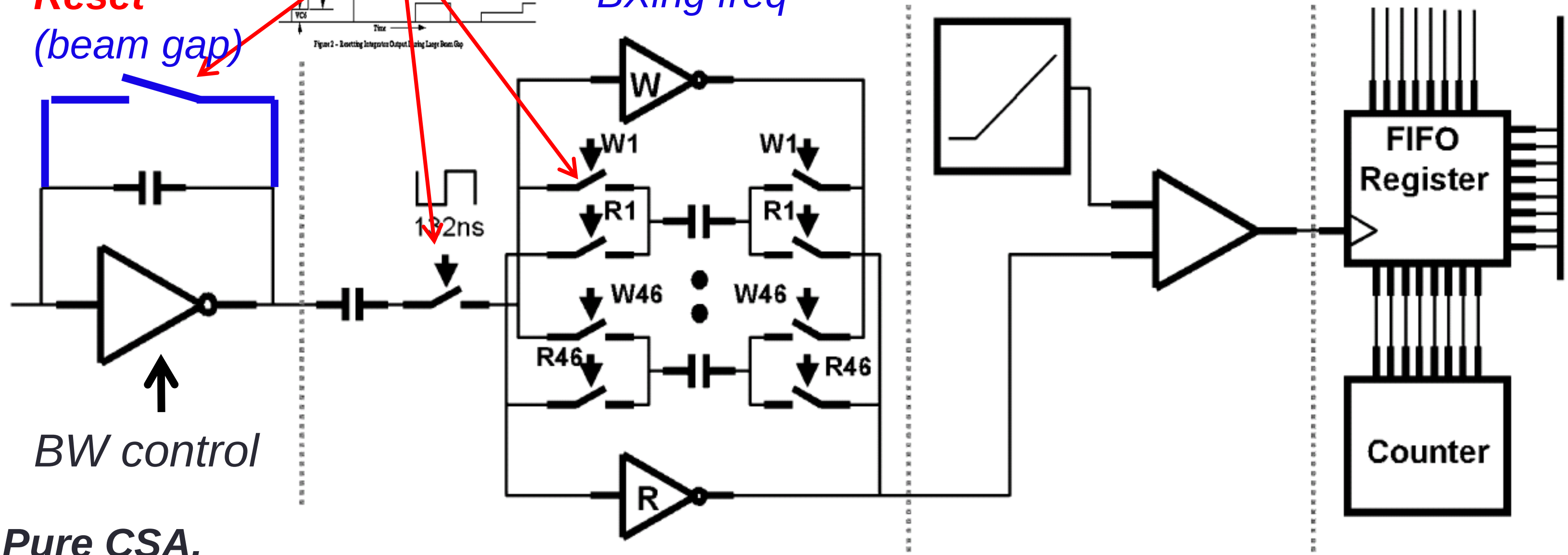


TSMC 0.25 µm, close-shape transistors (20 Mrad) : 6.3mm x 9 mm

Periodic Reset *(beam gap)*



CDS *+ 7 MHz sampling BXing freq*



// 8 bit
52 MHz
2V diff

BW control

Pure CSA,
no derivation
20-80ns risetime
200 fC *dynamic range*

SCA PIPELINE
46 cells L1 latency buffer, + event buffer (4 events)

Wilkinson ADC
8-bit 2x105 MHz
=> 1.2µs conversion

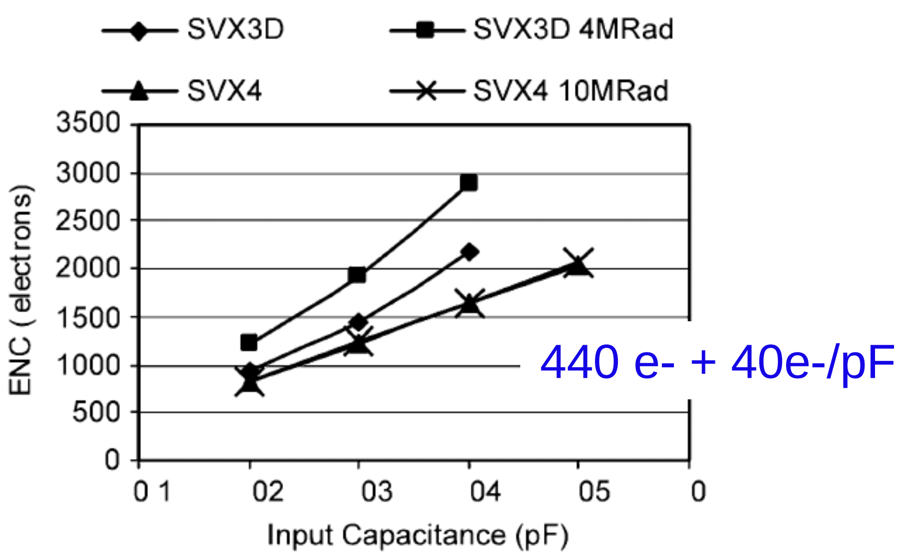
FIFO
Sparsified readout
Using shift register
Only data > thresh
or neighbours

SVX chips special features and performance

- Because of zero supression common mode noise is an issue => « RealTime Pedestal Supression »

- To cope with damaged strips: « Black Hole Elimination », Disable selected preamps but bias the input the proper voltage.

- 2 modes of operation:
    - CDF : simultaneous acquistion & digitization + RO
    - D0: deadtime during digitization & readout



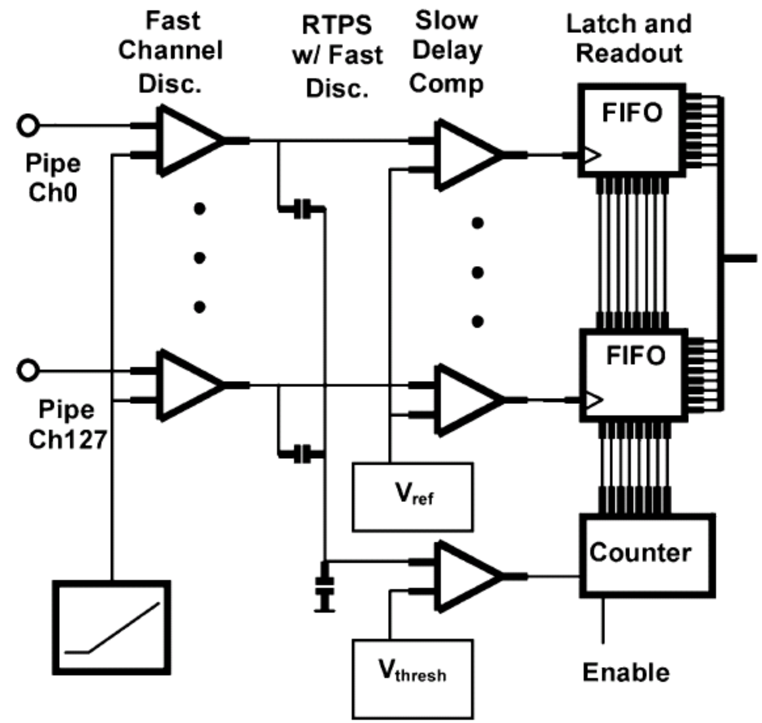
RTPS

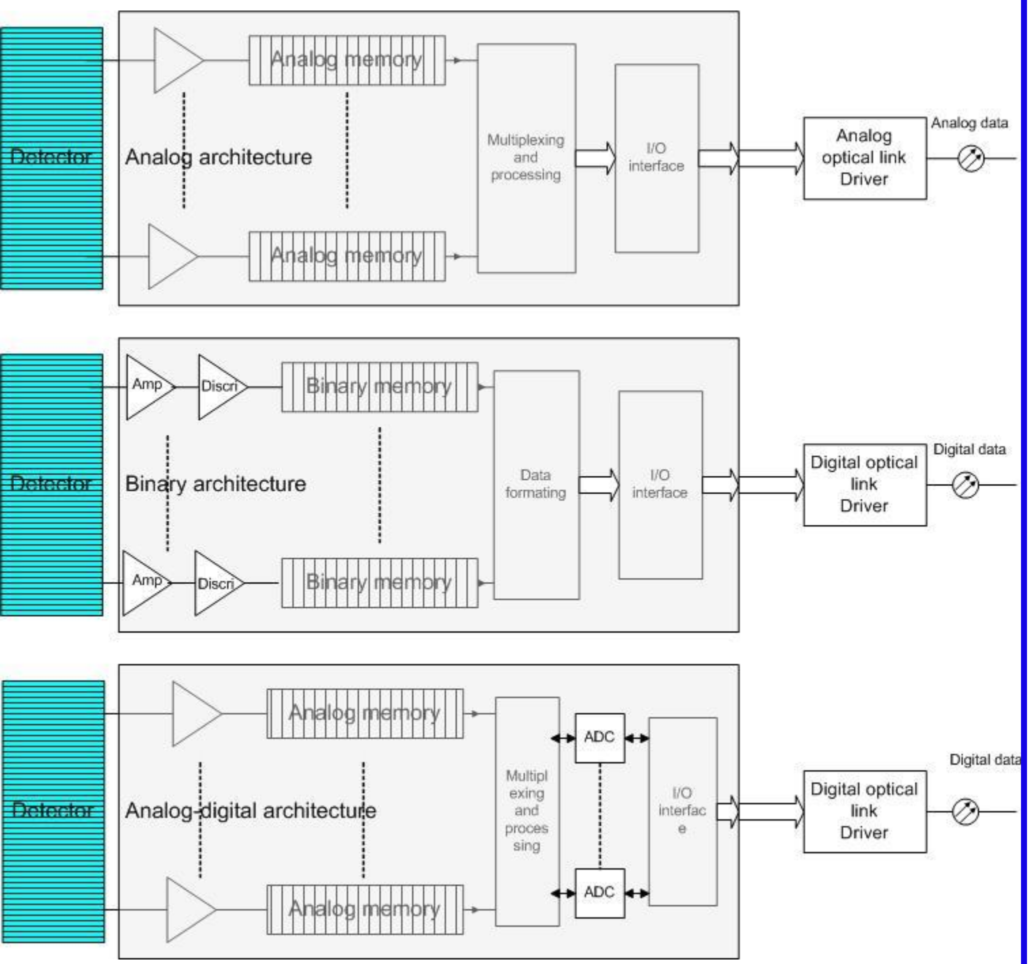
=> Fast comparators

Start the counter when n (typic 40) channels are converted.

= estimation of the common pedestal

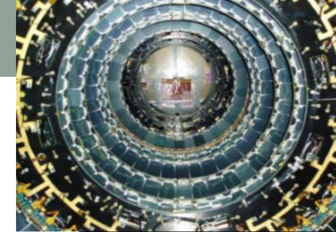
Slow comparators: give delay to measure properly the pedestals



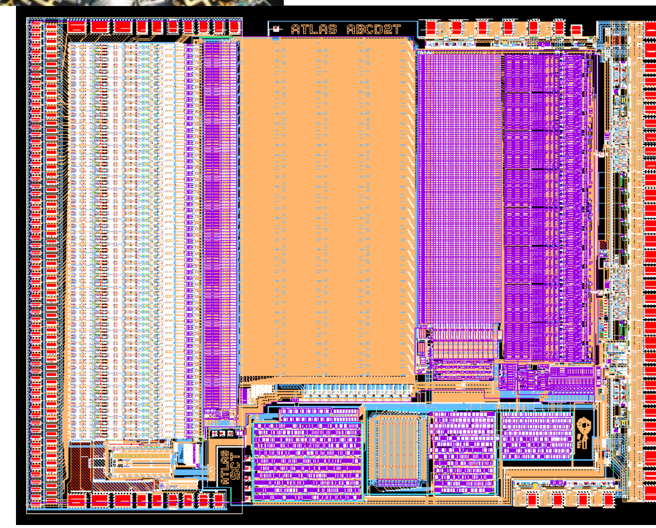


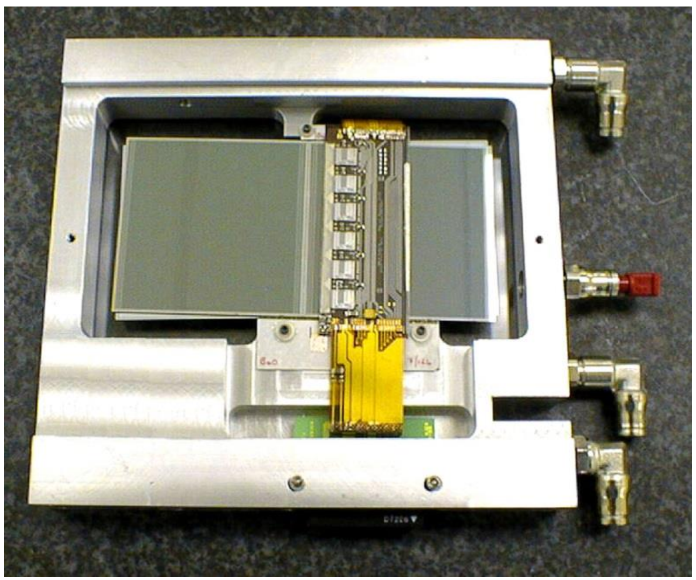
- **Analog CMS tracker APV25 radtol**
  - Charge sensitive amplifier
  - Analog memory 2us deep
  - Signal deconvolution
  - Analog multiplexing 128 channel
  - Serial analog optical transmission
- **Binary ATLAS ABCD3T DMILL**
  - Local hit decision
  - Preamplifier shaper discriminator
  - Digital memory 2.5us latency
  - Data formatting
  - serial digital transmission
- **Analog-digital ALICE PASCAL radtol**
  - Charge amplifier, shaper
  - Analog memory 4us
  - Readout of the full memory
  - On chip digitization 10bit 5 MSa/s
  - Serial digital transmission

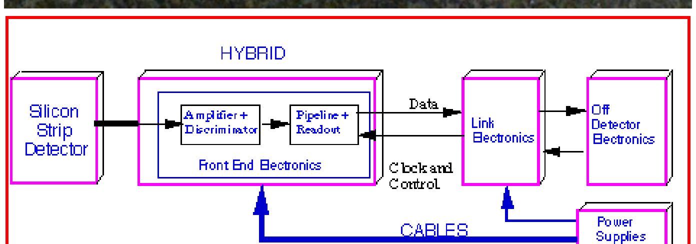
ATLAS silicon tracker: ABCD3

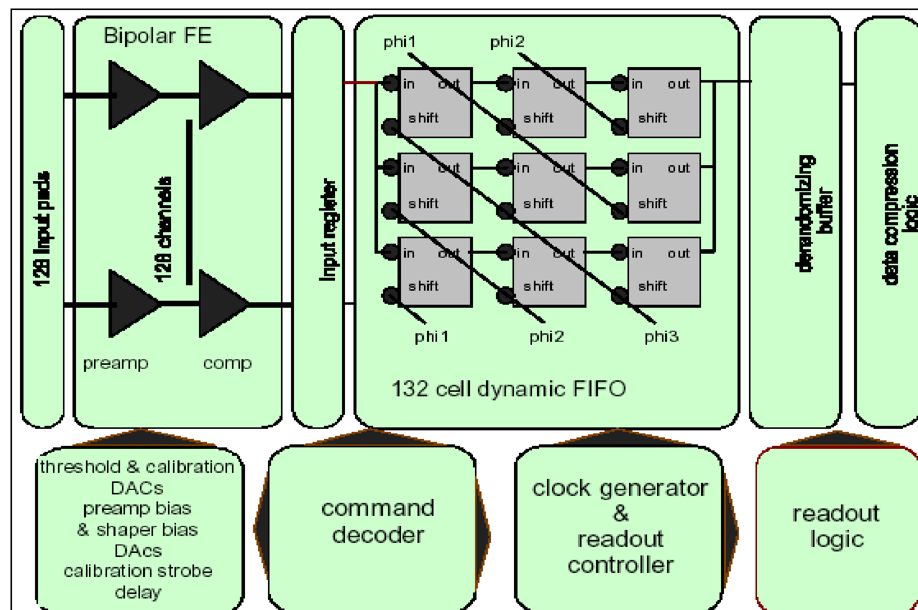


- » FRONTEND PREAMPLIFIER WITH BIPOLAR INPUT
- » 128 binary channels, 3.3uS 1 bit storage @ 40MHz
- »DMILL~ 30 000 bipolar's , ~ 200 000 MOS's
- » LVL1 DERANDOMIZER (8 EVENTS)
- » Data compression, errors and overflow handling
- » Serial 40Mbits input & output coding







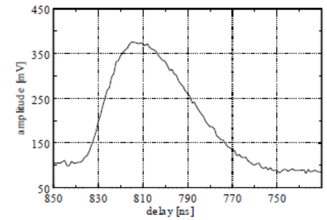


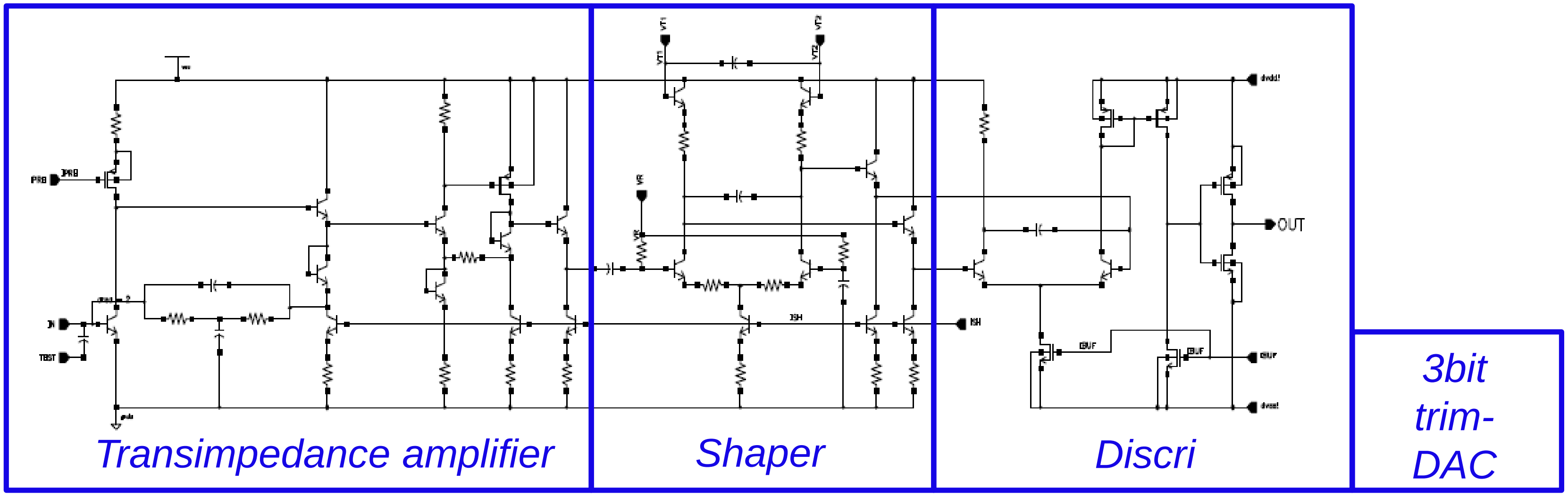
Solving the power consumption puzzle : ATLAS ABCD [ANG 97]

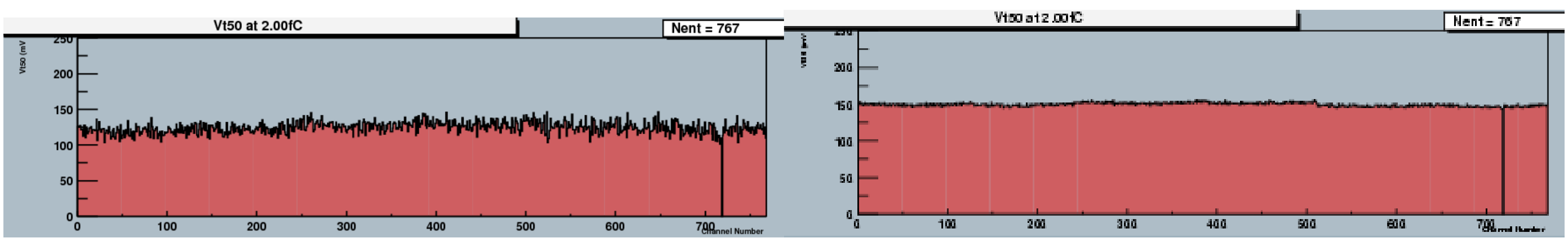
- Transimpedance input stage (see lesson of J. Kaplon 2011).

Part of the shaping (avoid one stage)

- BiCMOS technology (DMILL) : gm = IC/Ut, fast risetime good matching, Low serie noise (compared to 0.8µm technologies existing at this time







2fC Thresold voltage before trimming and after trimming

ATLAS ABCD : Use of Bipolar

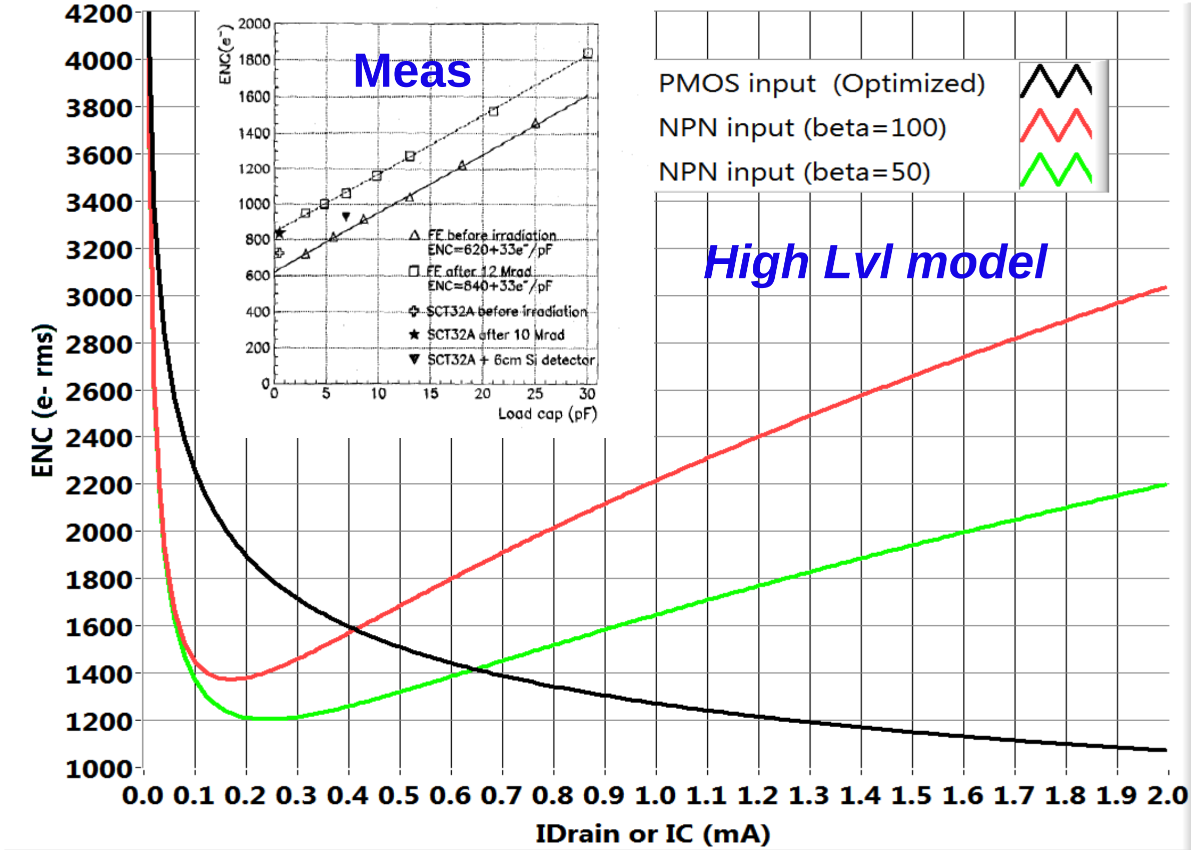
NPN

$$ENC = \sqrt{\frac{4kT\left(r_{bb} + \frac{kT}{2qI_c}\right)(C_a + C_d)^2}{T_p} + \frac{2qI_cT_p}{3\beta}}$$

MOS

$$ENC = \sqrt{\frac{4kT\frac{2\Gamma}{3g_m}(C_a + C_d)^2}{T_p}}$$

ENC for Cd= 20pF, tp =25ns, Rbase =50 Ohm

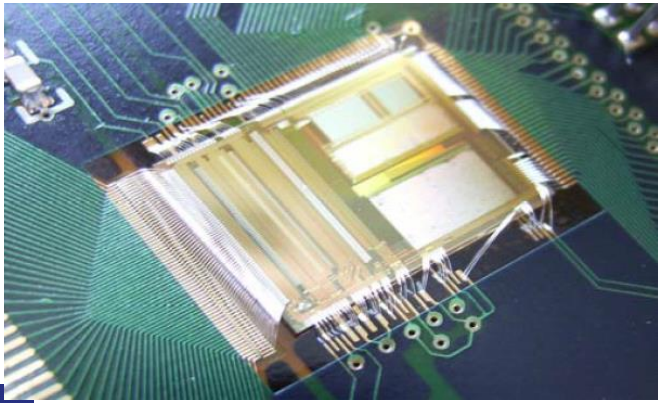


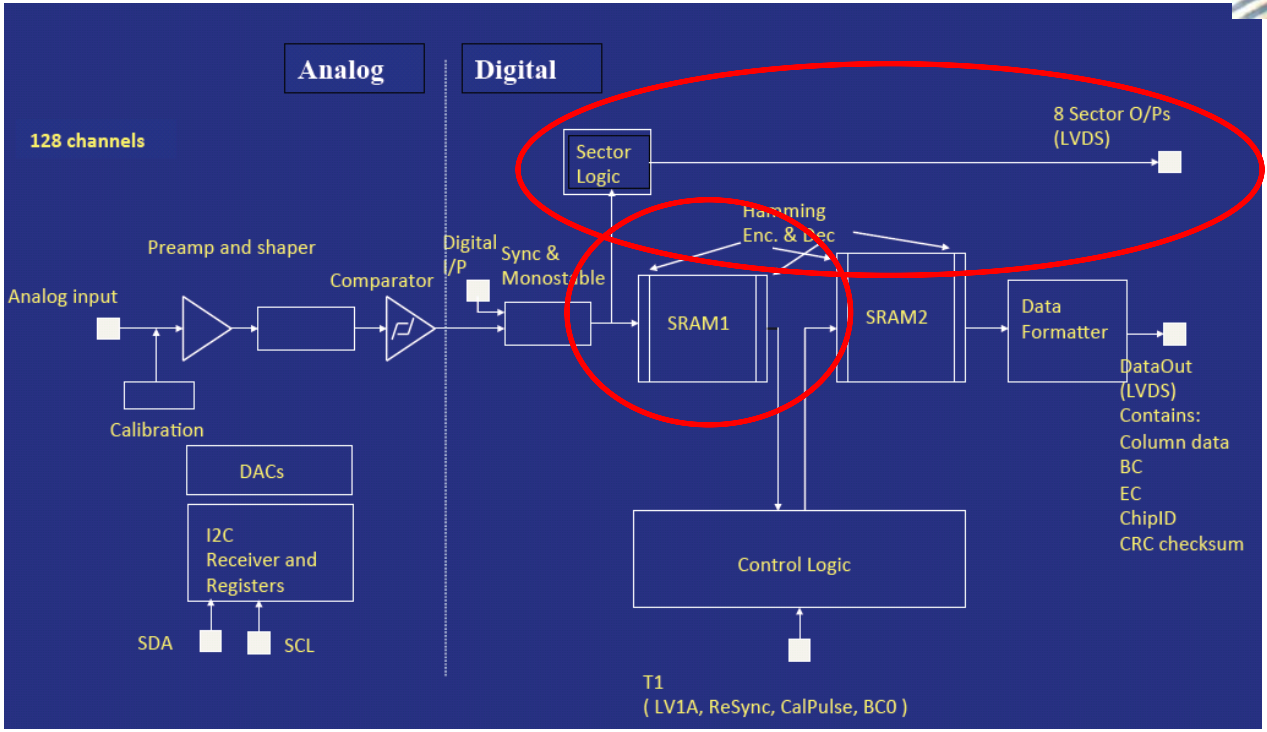
Lower noise for low power consumption for Bipolar transitors
Issue of NPN radiation hardness (gamma & neutrons)

Was true for 0.8µm CMOS node, less obvious for DSM CMOS

=> ABCN (HL-LHC) => pure CMOS 0.13µm or less

- Pure CMOS 0.25µm
- Use of standard RAM for Latency buffer





Fast sector-or output for trigger

Shaper order	CR-(RC)^3
Gain	60 mV/fC
Peaking Time	22ns
Linearity	± 12 fC
Input Impedance	120 to 200 ohm (at the central frequency)
GBW	600 MHz
Parallel Noise	400 e rms
Noise Slope	40 - 60 e/pF
ENC	1500 e (for an input cap. Of 20pF)
Time Walk	12ns (for signal 1.2fC to 10fC with a 1fC threshold)
Power consumption	1.5mW
Ionising radiation tolerance	Measured to 10 Mrad of Xrays with no observable effects.

From VFAT2 to ABCN

- VFAT 2[KAP 05]

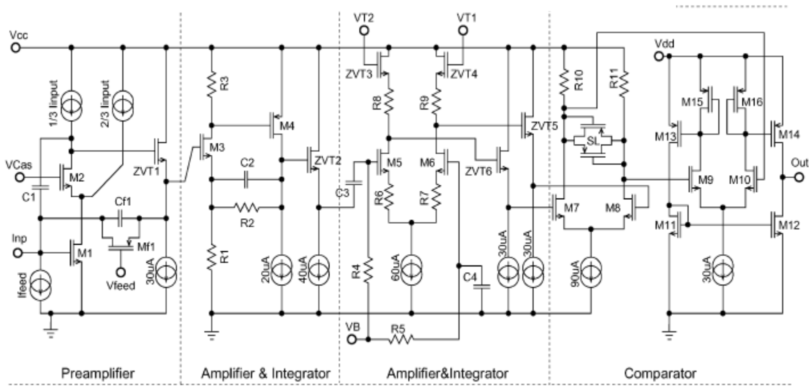
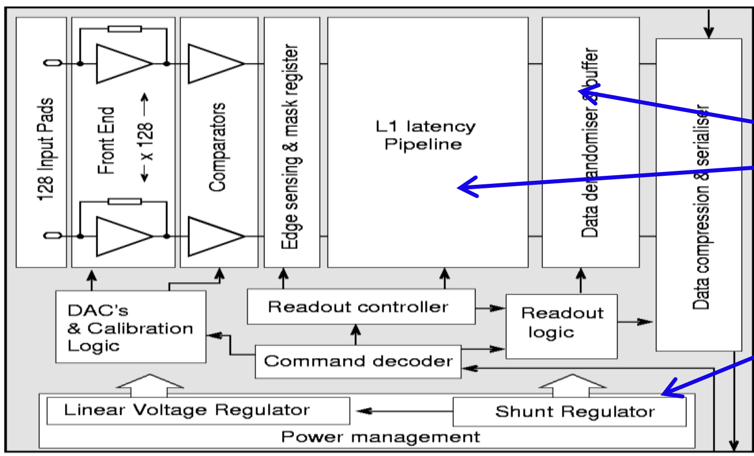
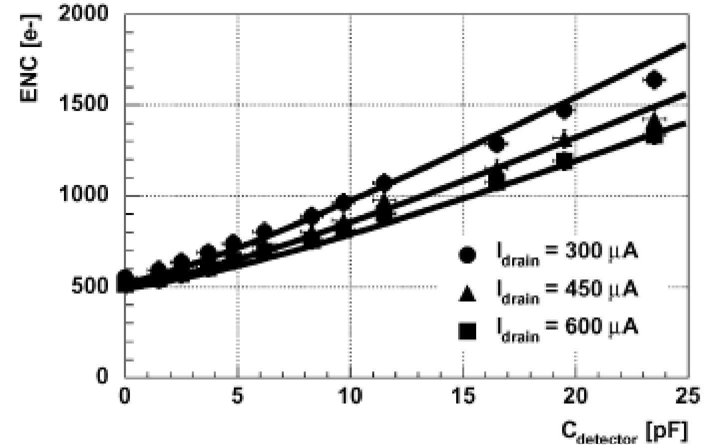


Fig. 1. Schematic diagram of one channel of the ABCDC1 chip.





CMOS is now more competitive

Memories are now standard blocks

On chip regulators

- ABCN 0.13µm see 2011 lesson of J. Kaplon

  * gm of NMOS input device (weak inversion) is only 25% lower than NPN,

  * no Rb !

  * Gamma of NMOS is good =1.3

- Simultaneous Write and read clocks run for level 1 event selection without dead time

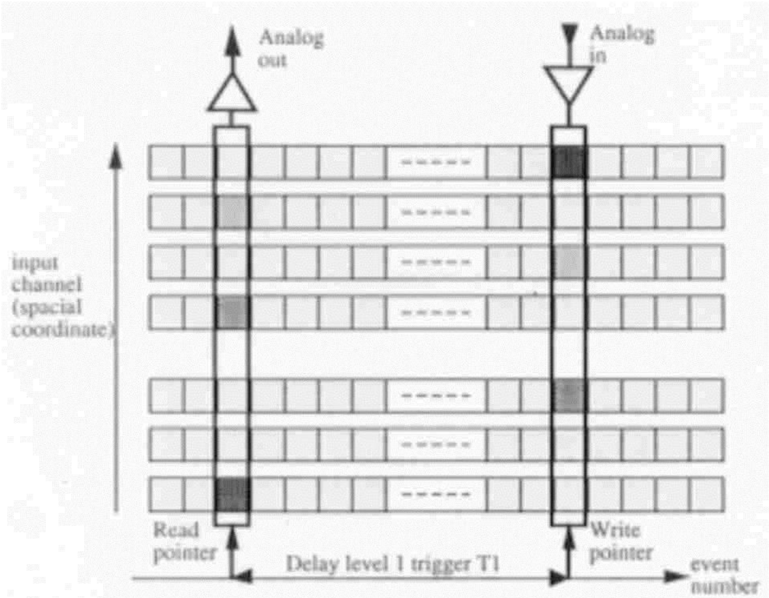
  - Write and read clocks run sequentially for retrieving all data from analog memory

  - sampling and storing analog signal controlled by LHC master clock (40 Mhz)

- Analog data retrieved by level 1 trigger

  - Columns belonging to a trigger time slot reserved for readout

  - Several columns can be simultaneously reserved for buffering several

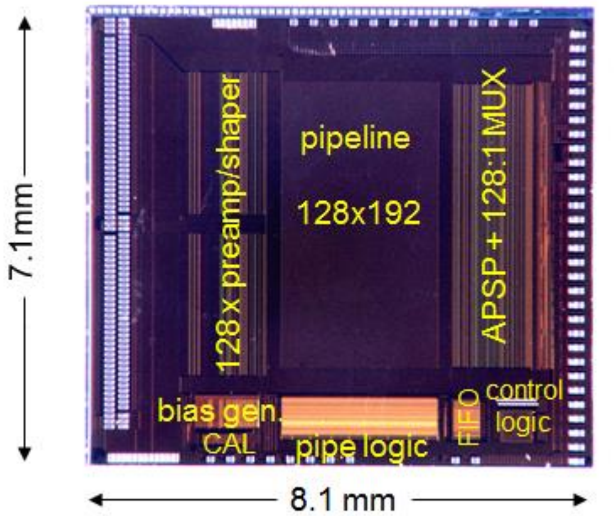


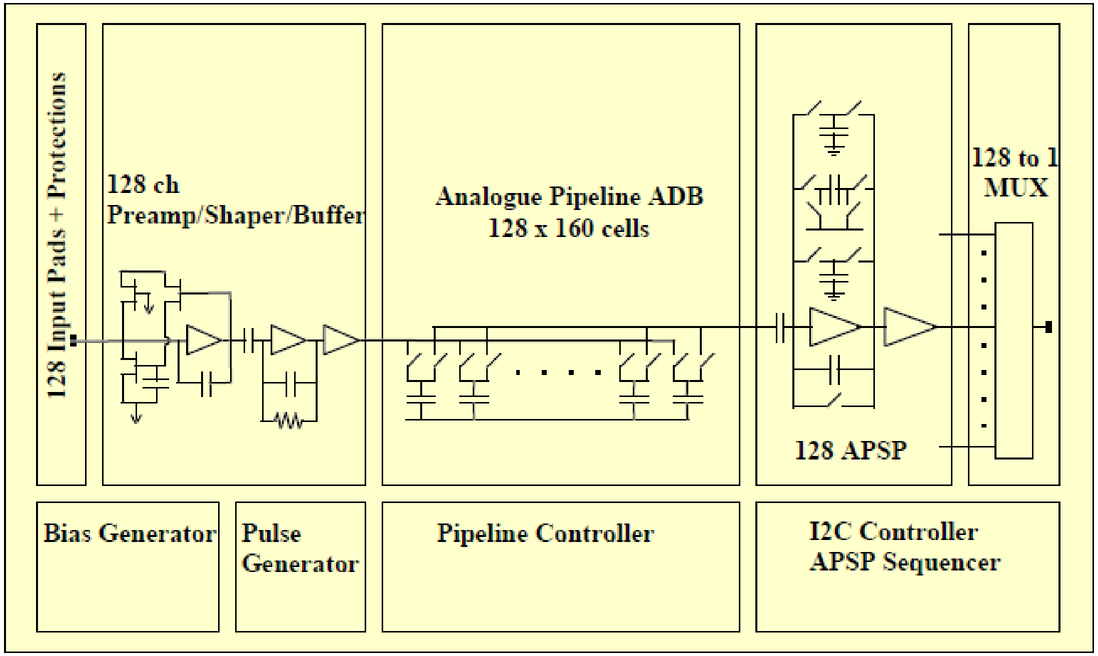
-Write and read clocks control write and read pointers

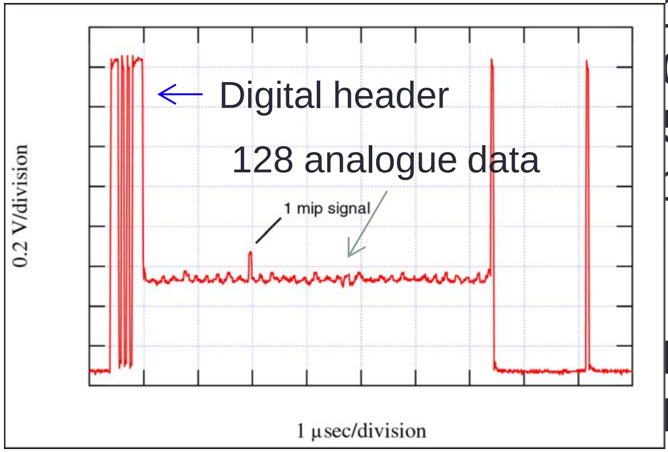
- Delay between write and read pointers adjusted to trigger 1 latency

-Analog memory maps data in time and space dimensions

CMS strip readout ASIC : APV25







128 channels: 2mW/ch

0.25µm IBM technology (>50 Mrads)

50 nsec. CR-RC shaper/amplifier

192 cell 40-MHz analog pipeline for:

4µsec L1 latency + buffering)

up to 32 event buffering

Peak/deconvolution operating mode

Embedded common mode subtraction system

Differential current buffer, 20 or 40MHz readout

I^2C slow control interface

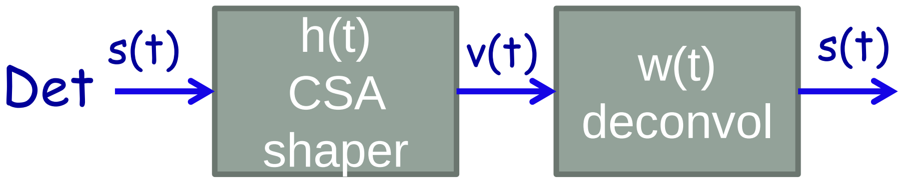
On-chip CAL circuit: amplitude and delay programmable

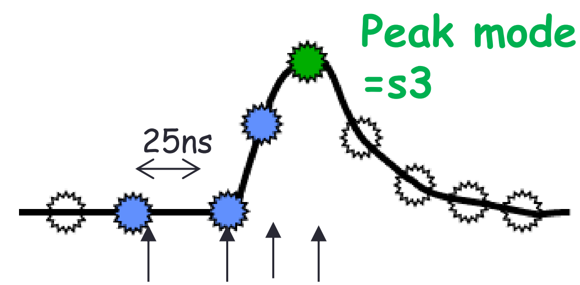
Rad-Hard: >>10 Mrads

No on-chip zero supress

1 value/ch/trigger

An other way to save power : Deconvolution [BIN93]





Deconvol = w0.S0+w1.s1+w2.s2

Convolution: $v(t) = \int_{-\infty}^{t} h(t-t')s(t')\,dt'$

For sampled signals $V_i = \sum_j H_{ij} S_j$ or $V = H \cdot S.$

Deconvolution Filter W $S = W \cdot V = H^{-1} \cdot H \cdot S$

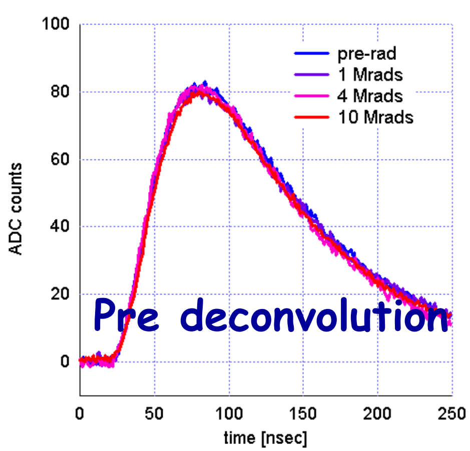
$$|W| = |H|^{-1} = \begin{bmatrix} w_1 & 0 & 0 & 0 \\ w_2 & w_1 & 0 & 0 \\ w_3 & w_2 & w_1 & 0 \\ . & . & . & . \end{bmatrix}$$

A simple matrix inversion operation ??

Usually, no simple exact solution => requires a lot of samples (infinite)

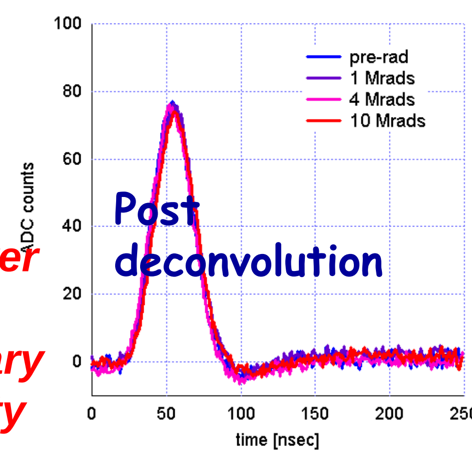
But for CR-RC filter, very simple and exact solution:

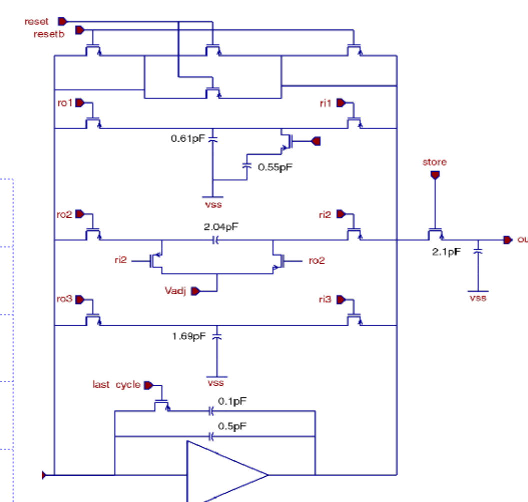
=> Very simple FIR with only 3 weights



Equivalent to fast FE with less power

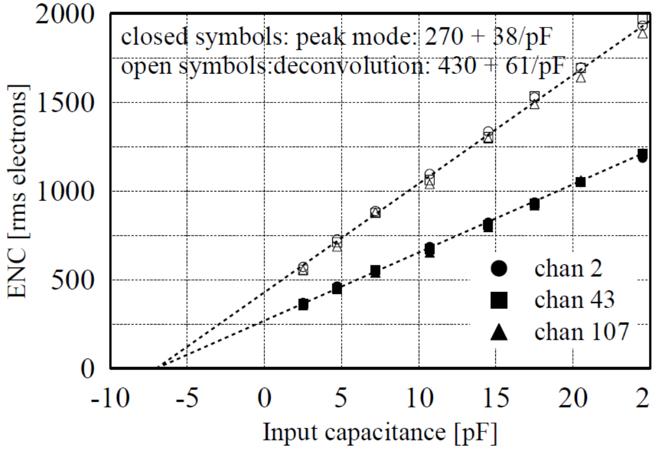
$\Rightarrow$ *BX Id. necessary for high luminosity*

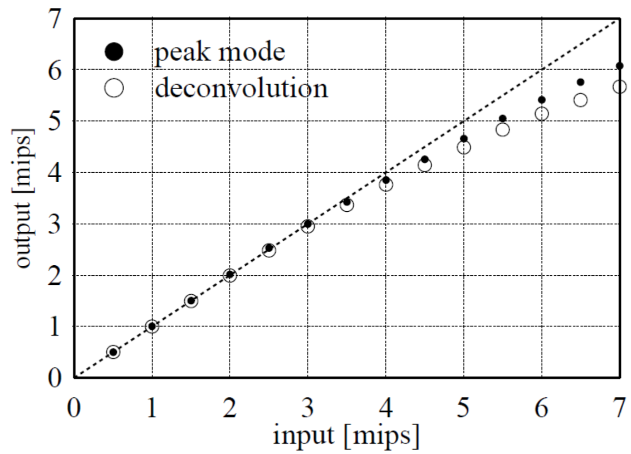


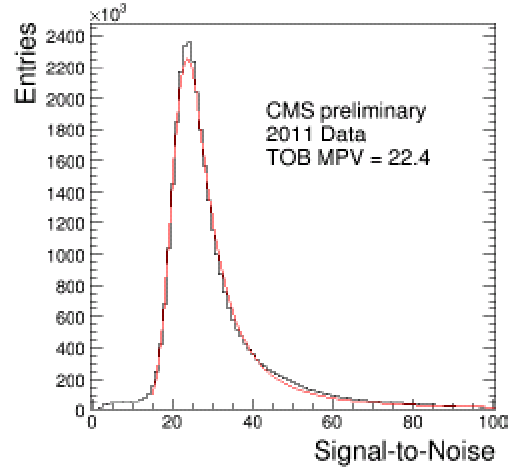


Switched Capacitor deconvolution

APV performance and APV “hijacking”



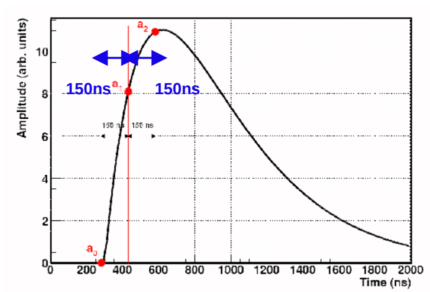


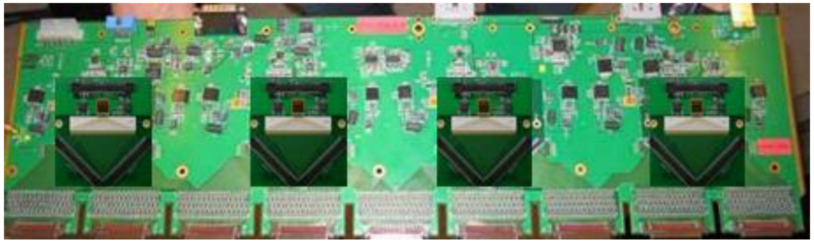


S/B In real environment (thick sensors)

A lot of parameters can be varied (ie peak time)
Usable with other detectors (Compass GEM tracker (TUM)):

- Now popular in the gazeous detectors community with modified readout.
- Exemple: [ABB07] for MWPCs of COMPASS Rich
  - 300 ns peak time
  - Common mode noise suppression
  - 40 MHz operation
  - Timing using thres150ns-spaced samples
  - Pile-up rejection using the samples

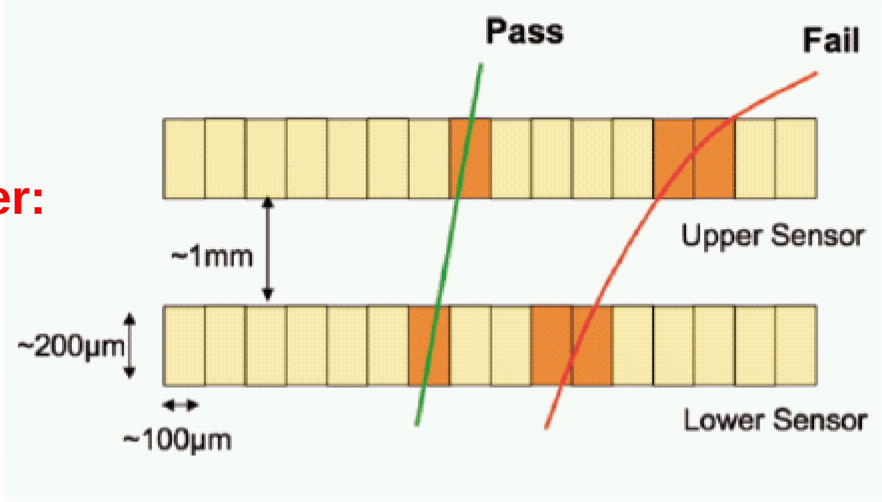




- Shorter strips for Less Occupancy
- Binary solution for easier interfaces
- Limit the trigger rate to 100kHz =>

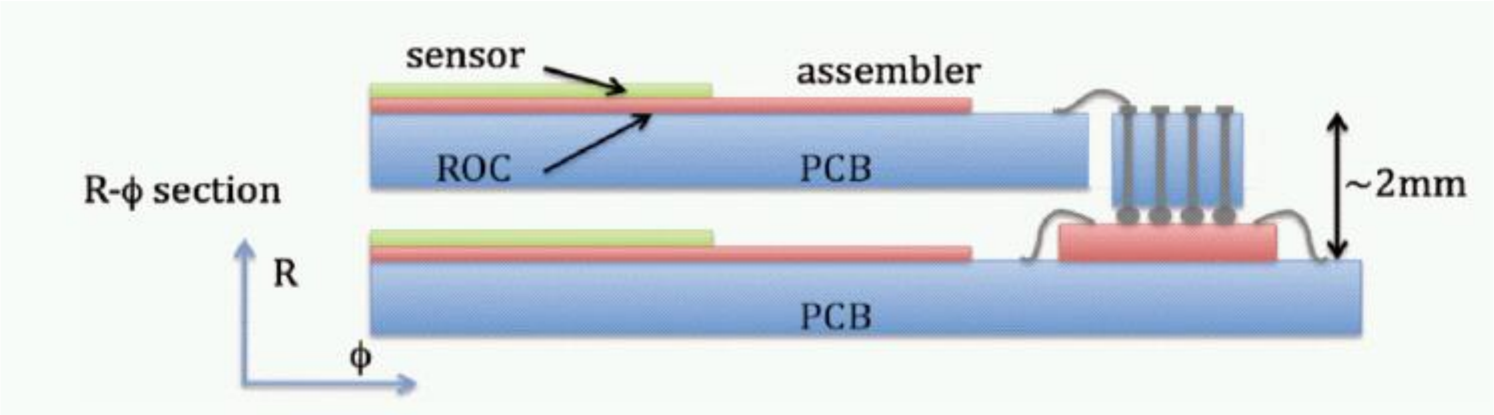
Tracker now participates to the L1 trigger:

- Higgs golden channel : H→ZZ →4µ
- No interest for low momentum tracks
- Trigger on high momentum tracks
- Deduce particle momentum from track curvature In the Tracker

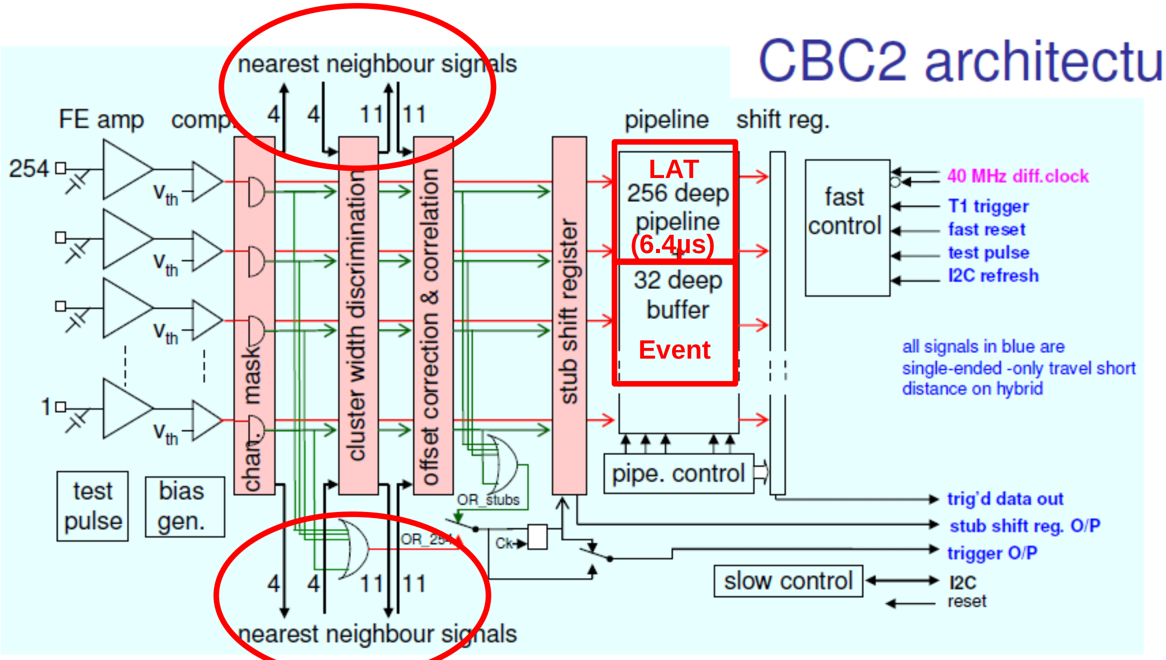


⇒ **Concept of PT module**

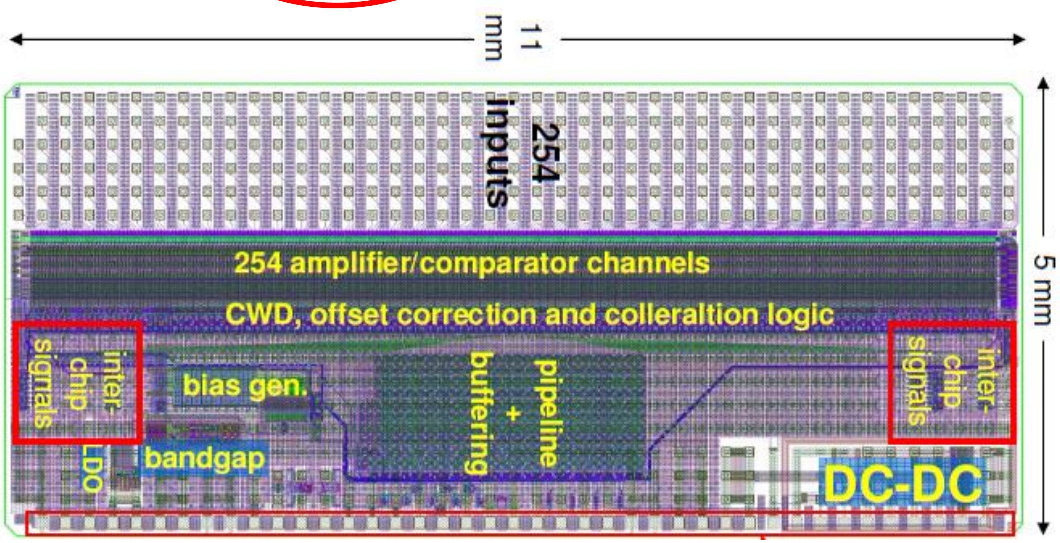
⇒ Need immediate tagging of interesting tracks.

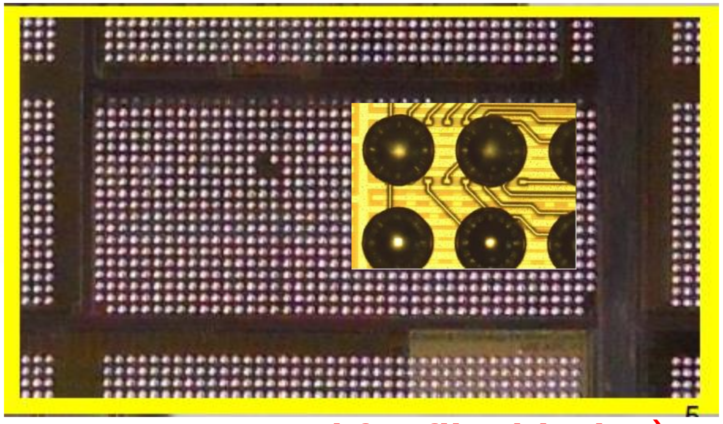


CBC2 architecture

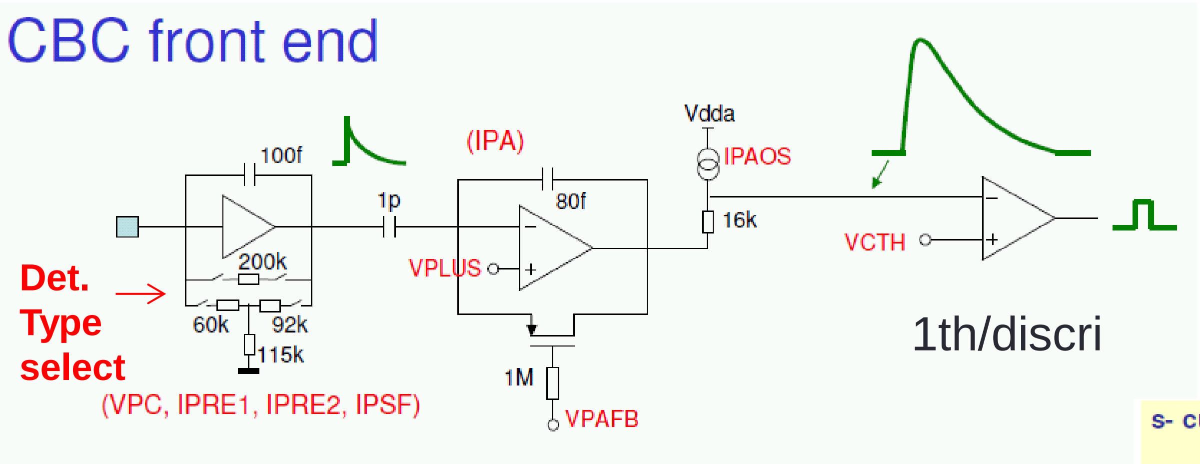


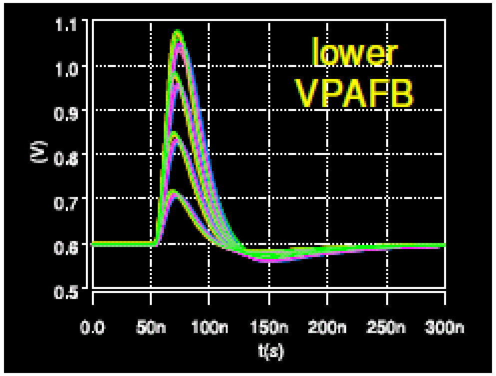
- IBM 0.13
- 254 channels.
- ASD + buffer
- FlipChip
- On-chip DC-DC & LDO
  2.5V->1.2V for core
- Include Pt functionalities
- Fast Output for trigger
- Differential SLVS signals



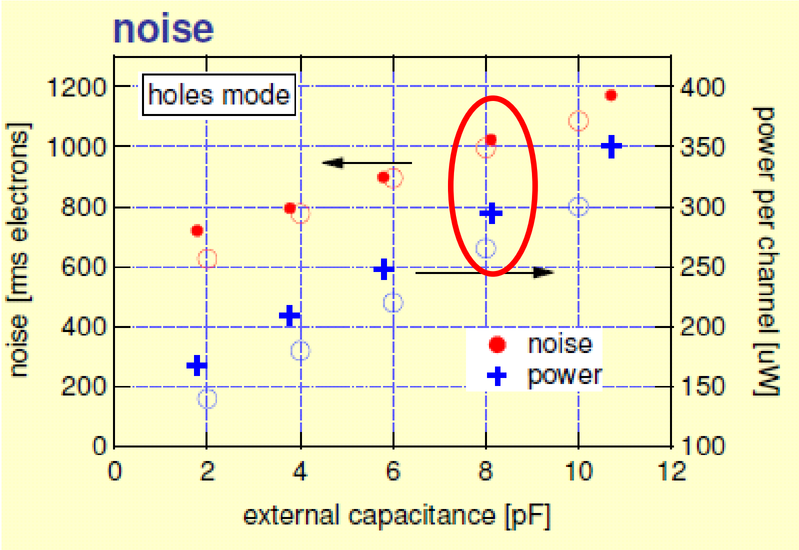


CBC2 prepared for flipchip (C4)

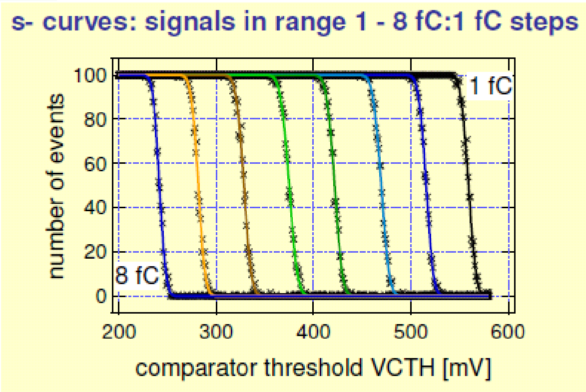


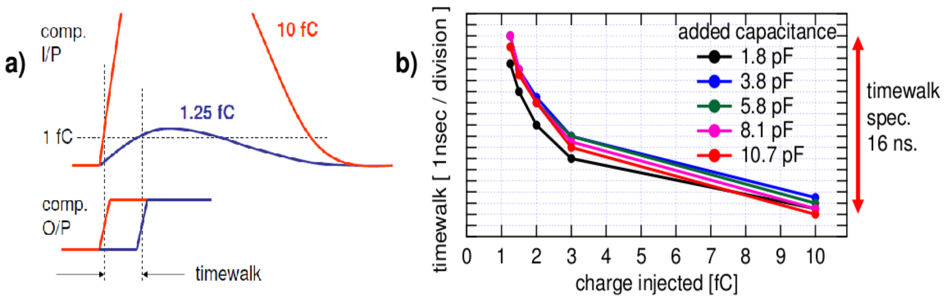


<50ns width for Q<2fC



1000e- for 8pF/ 350µW





stub finding logic

cluster width discrimination (CWD) logic

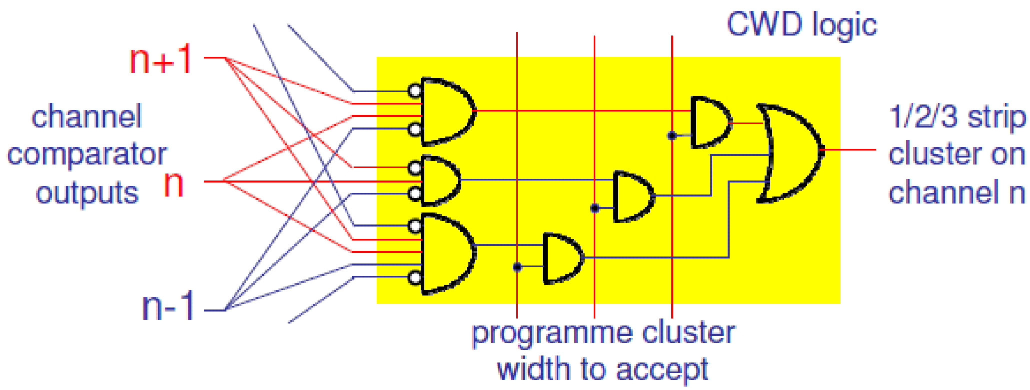
exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

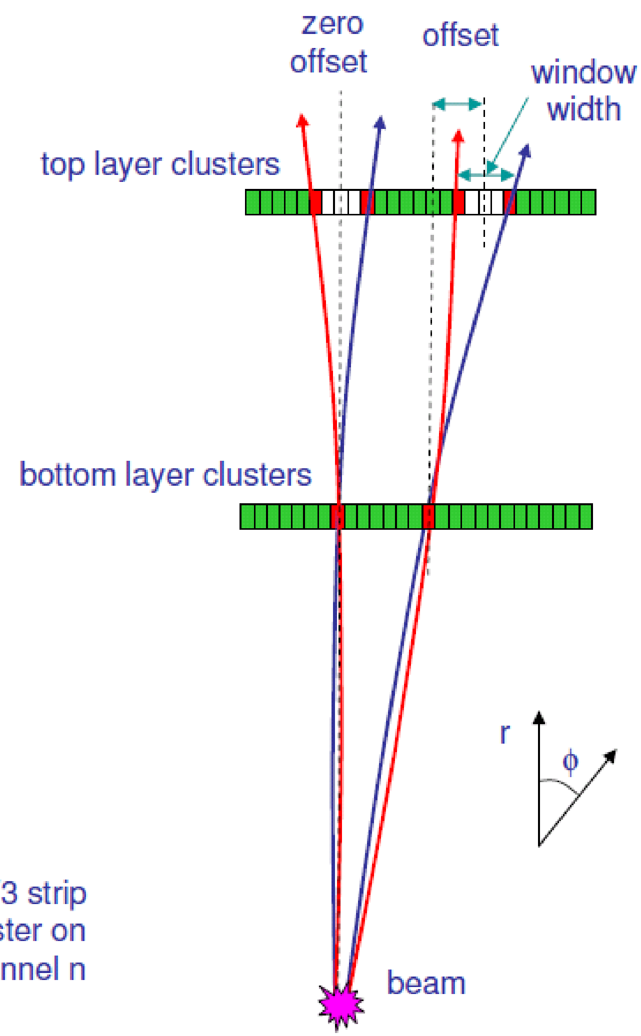
offset correction & correlation logic

for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

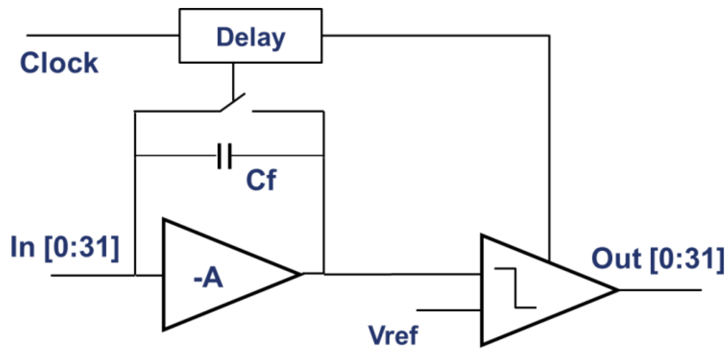
window width controls pT cut
stub found if cluster in bottom layer corresponds to cluster within window in top layer
window width programmable up to **+**/- **8** channels

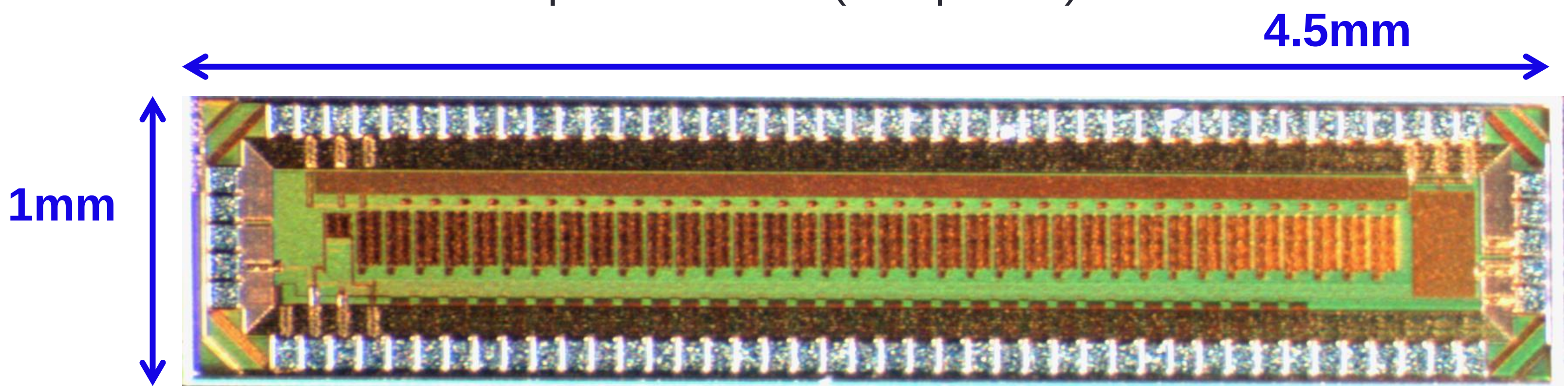
offset defines lateral displacement of window across chip
programmable up to **+**/- **3** channels





- IBM 0.13µm
- Based on switched-preamp.
- Dead-Time reduced to 25ns
- 300 µW/ch
- Promising results on first prototype:
  - ENC = 580 e- + 120 e-/pF (15 MHz CK)
- 32-channel FE chip under tests (see poster).

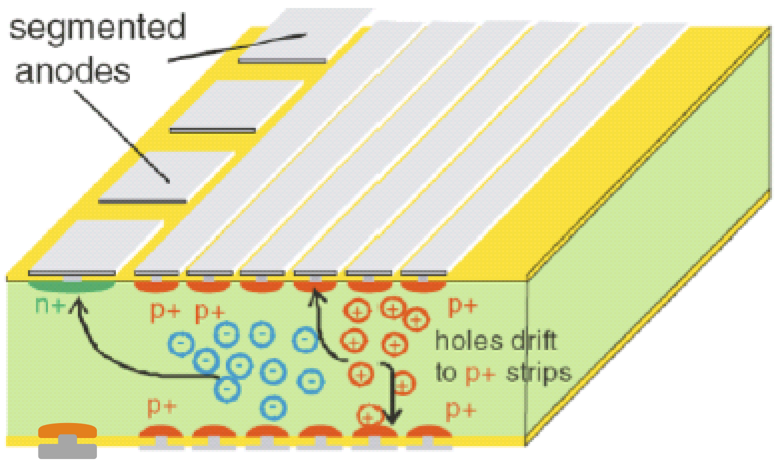




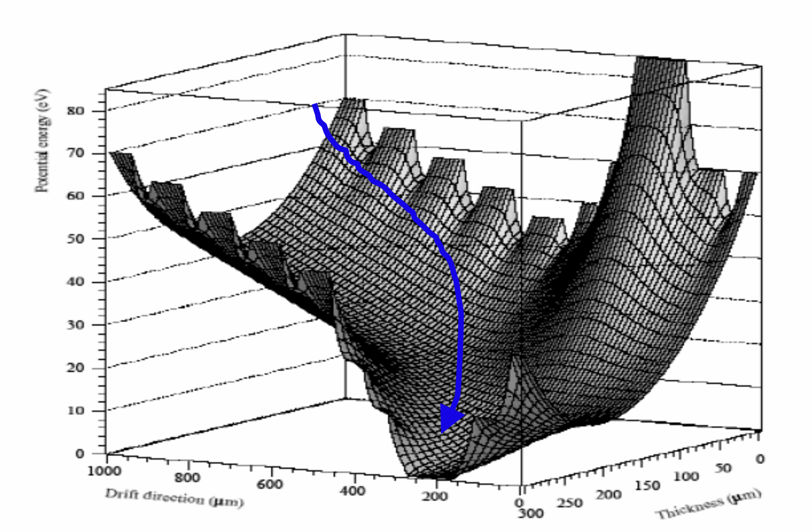
- MiCRHAU is also involved in data concentration

Principle of the Silicon Drift Detector (SDD)

Evolution of Silicon Sensor Technology in Particle Physics, F. Hartmann, Springer Volume 231, 2009



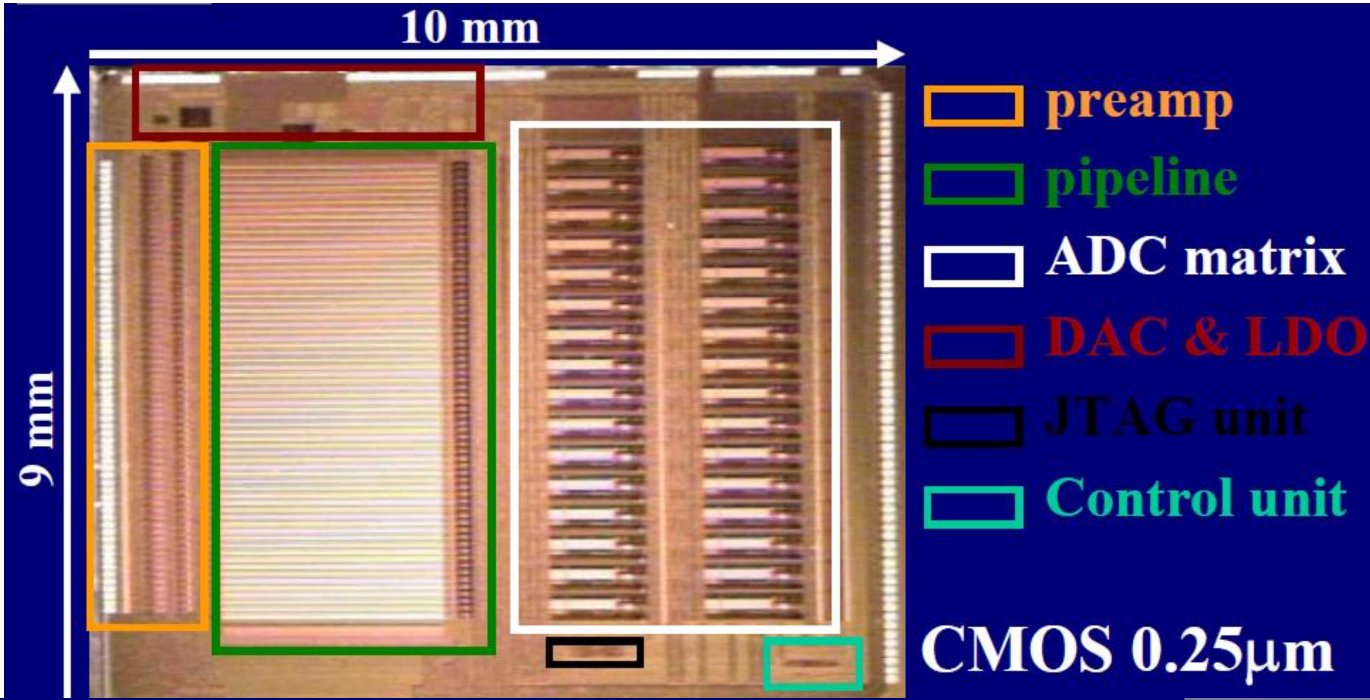
P+ Cathods on both side of the wafer : Depletion of the Silicon
|HV| decreases toward the anods
→ Drift field => collection
Last cathods below the anods potential

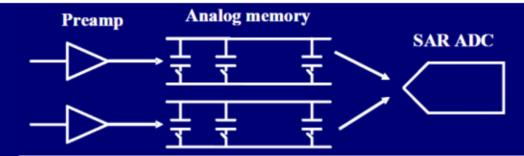


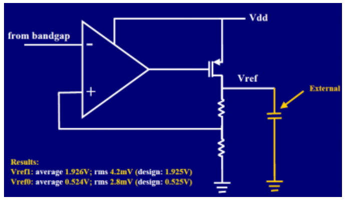
Potential inside the SDD
« Tobogan » effect

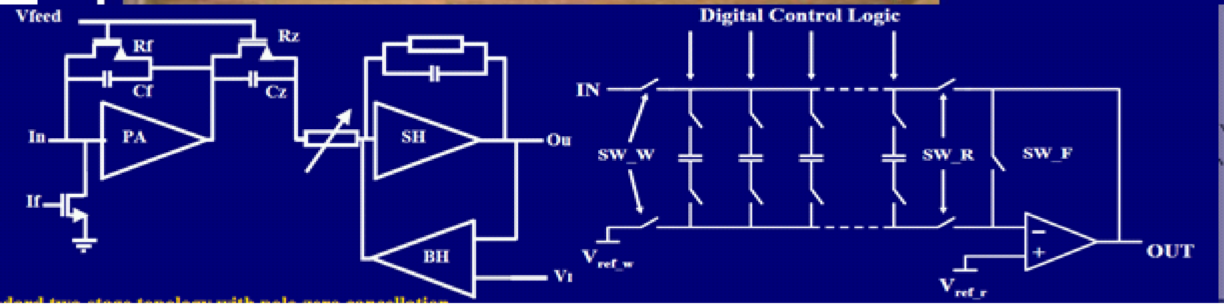
- **2D readout with single measurement**
- **Low capacitance (anode only) for a large detector surface.**
- **Position reconstruction :**
  - Centroid calculation
  - Position X : anods
  - Position Y : drift time (T dependency)
  - dE/dx : Integral of the signal

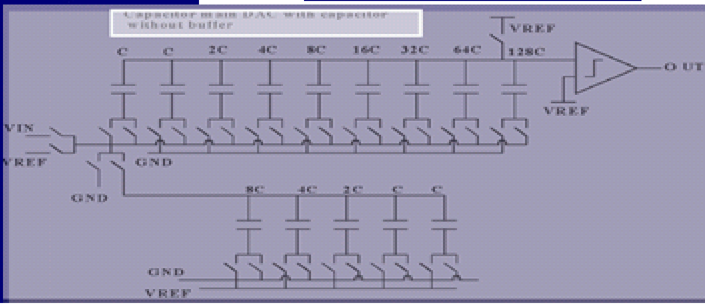
Requires waveform sampling of all the drift ~6µs







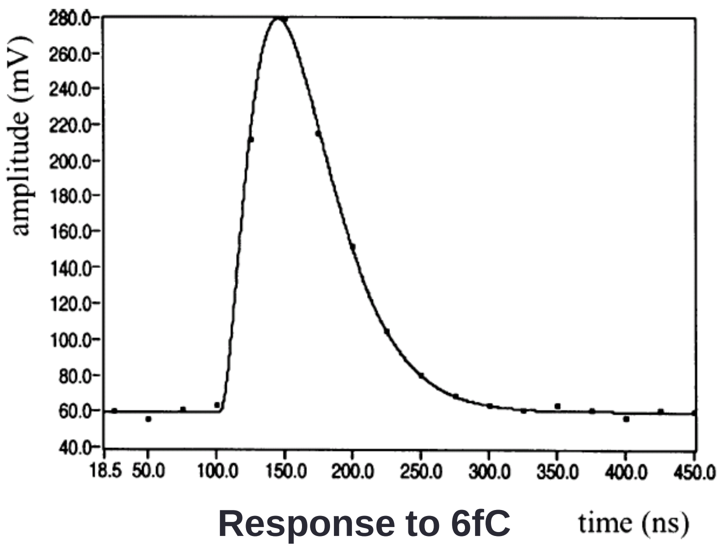




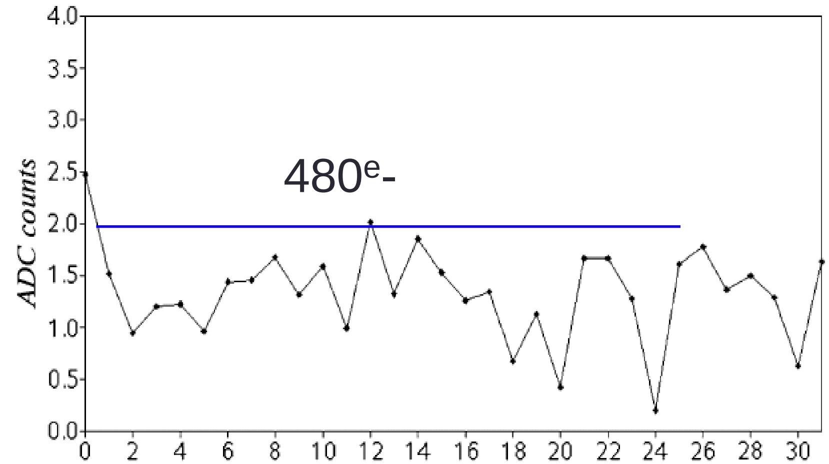
- 64 ch (IBM 0.25)
- Preamplifier shaper 40ns peaking time
- Analog memory 256 cells deep x 64 channels
- 40MSPS writing speed
- 32 x 10bit SAR ADC 4Msamples/s ADC

- Everything read/ each trigger: 380-1000μs
- AMBRA companion chip (data reduction)
- Internal LDO for reference
- 9mW/ch (4mW for core only)
- ENC with detector = 250 e-rms (Low CD)

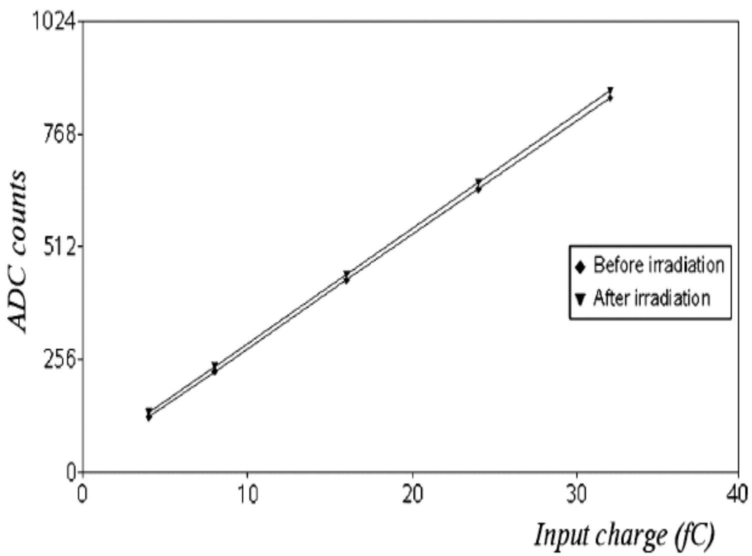
Pascal for ALICE SDD: performance



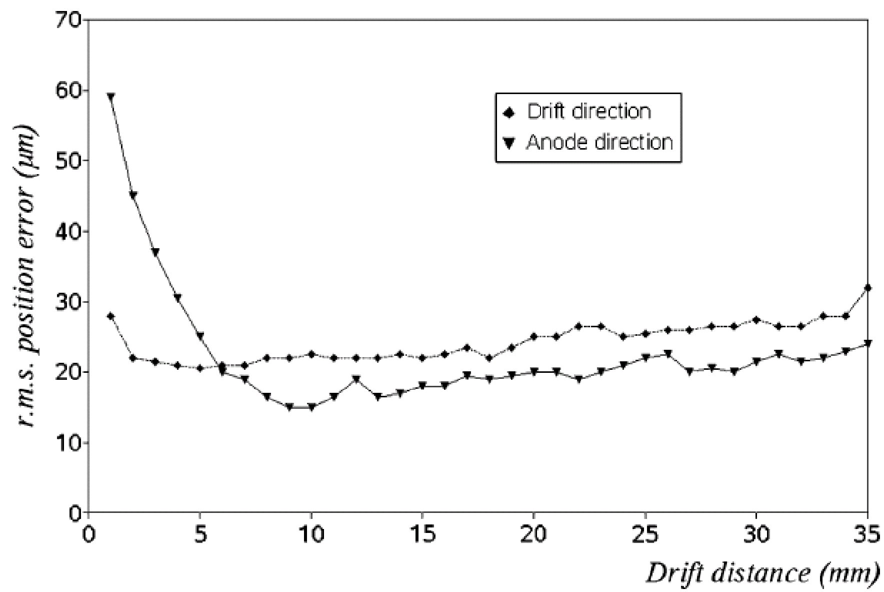
Response to 6fC



noise

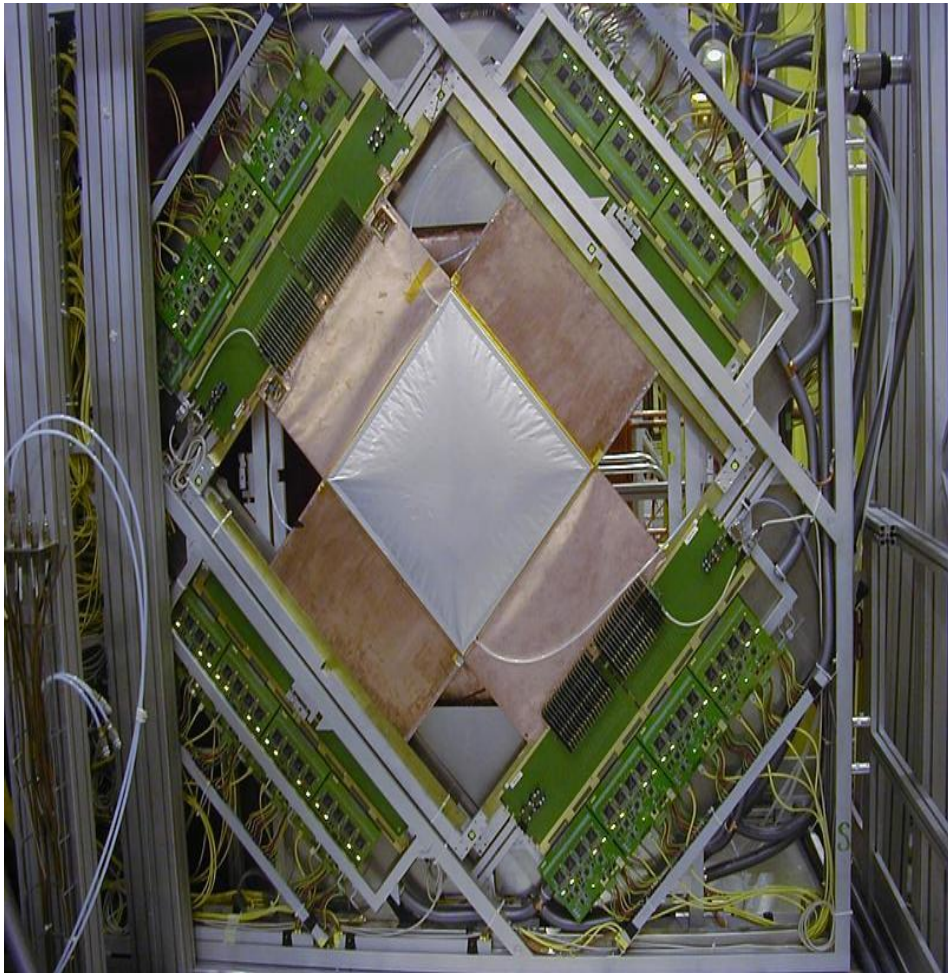


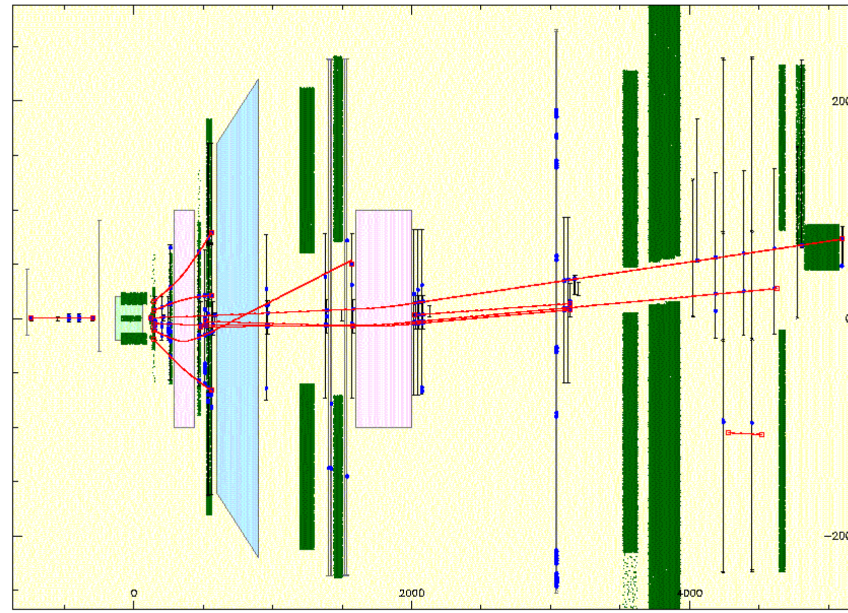
Transfer Function before and after 30 Mrad



Position resolution with SDD

Gazeous detectors

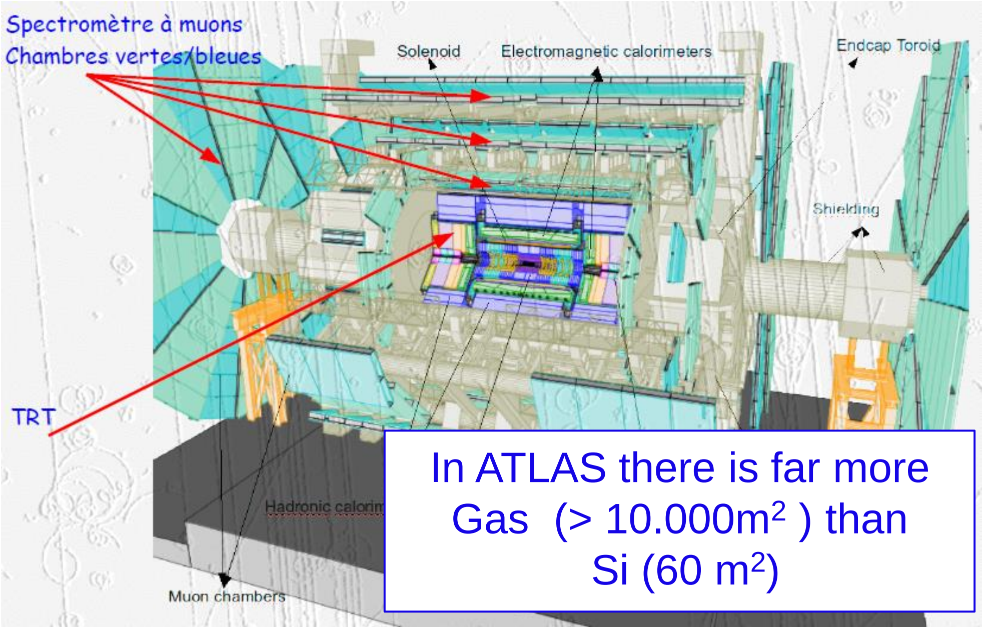




Si vs Gas (MPGD)

	Si	Gas
Cost	☹	☺
Material budget	😐☹	☺;TPC☺☺
Ionisation	☺	☹
Cdet	😐	☺
S/N	☺	☺(Gain)
Spatial Res	☺ (µms)	😐 (50µm)
E resol	☺	😐
Rate	☺	☺ (MPGD)
Timing	☺ (ns)	☺😐
Infrasctucture	☺ ☹cooling	☹ (gas)
Rad. Hard.	☹	☺
Cost	☹	☺

Gas is well adpated to large volume detectors with moderate requirement for spatial resolution



In ATLAS there is far more Gas (> 10.000m^2) than Si (60 m^2)

Wire Chambers: principle

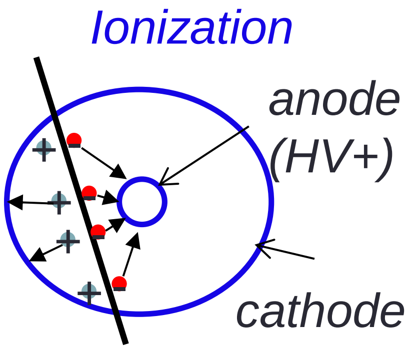
- ~ tens of e-/ion pairs created by ionisation in gas (4 order of magnitude less than in Si !
- E field proportional to 1/r
  - High field near the wire.
  - Mulitplication by $10^4 – 10^5$
  - Limited by sparks
- Ion drift to the cathod
  - hyperbolicSignal induced in both electrod

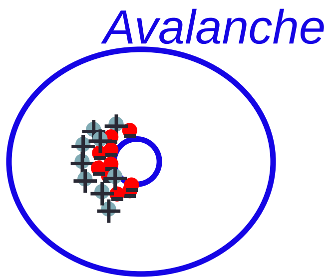
$$i(t) = \frac{q}{2t_0 \ln\frac{b}{a}} \frac{1}{1+t/t_0} = I_0 \frac{1}{1+t/t_0}$$

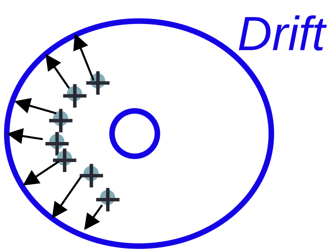
  - Long ion tail (up to µs), usually cut by shaping
    => Ballistic deficit, often <50% of the charge is used
  - Large density of charge (ion) in the gaz
    => space charge limit at high rate
  - **Tail and ion density problems no more existing in MPGD**
- Very small capacitance for wires
  ⇒ Large detector with high S/N
- Charge statistics = ionization (Poisson) convoluted Avalanche statistics (POLYA or Fury exp distribution): E resolution Not as good as with Si.

Here it is the simplest wire chamber Proportional counter.
A lot of more complex and samart designs, but based on the same principle:
- MWPC (Charpak)
- Wire or cathod plane (strips or pads) readout

* Drift Chambers
…..

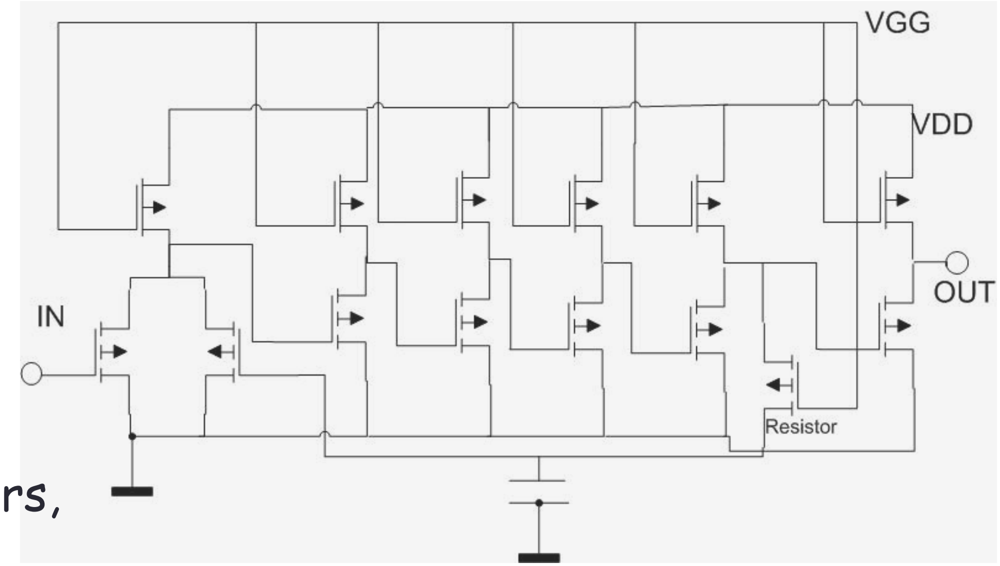






FILAS : 1974

- ✓For MWPCs
- ✓A revolution !
- ✓Still in use in late 80s
- ✓Only PMOS technology (EFCIS)
- ✓8 Channels
- ✓Ampli + discri
- ✓Cascade of 6 stages of x 3 amplifiers,
- ✓No cascode
- ✓ 0.2 W/ch
- ✓Noise = 20 000 e-



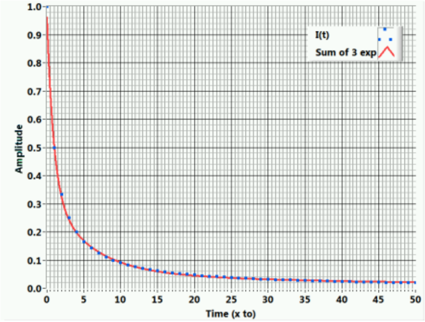
Ion Tail cancellation [BOI82]

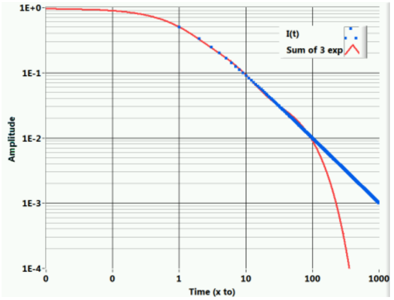
$$i(t) = \frac{q}{2t_0 \ln \frac{b}{a}} \frac{1}{1+t/t_0} = I_0 \frac{1}{1+t/t_0}$$

- ✓ Current is
- ✓If use of CRx-RCn shapers => long overshoot or tail
- ✓ Sometimes ok.
- ✓ If high rate => pile-up => rate dependant baseline shifts.
- ✓Ion tail cancellation is required.
- ✓Idea: approximate the signal by a sum of exponentials (the more is the better),

$$i(t) \simeq I_0 \sum_{n=1}^{N} A_n e^{-\alpha_n t/t_0} = I_0 \sum_{n=1}^{N} A_n e^{-t/\tau_n} \qquad \tau_n < \tau_{n+1}.$$

- ✓3 is usually enough,
- ✓After Laplace transform



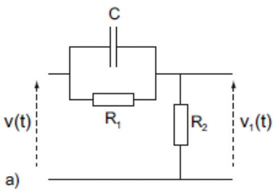


$$\sum_{n=1}^{3} \frac{A_n}{s+1/\tau_n} = \frac{as^2+bs+c}{(s+1/\tau_1)(s+1/\tau_2)(s+1/\tau_3)}$$

$$I(s) \simeq I_0 \frac{a}{(s+1/\tau_1)} \frac{(s+1/\tau_a)}{(s+1/\tau_2)} \frac{(s+1/\tau_b)}{(s+1/\tau_3)}.$$

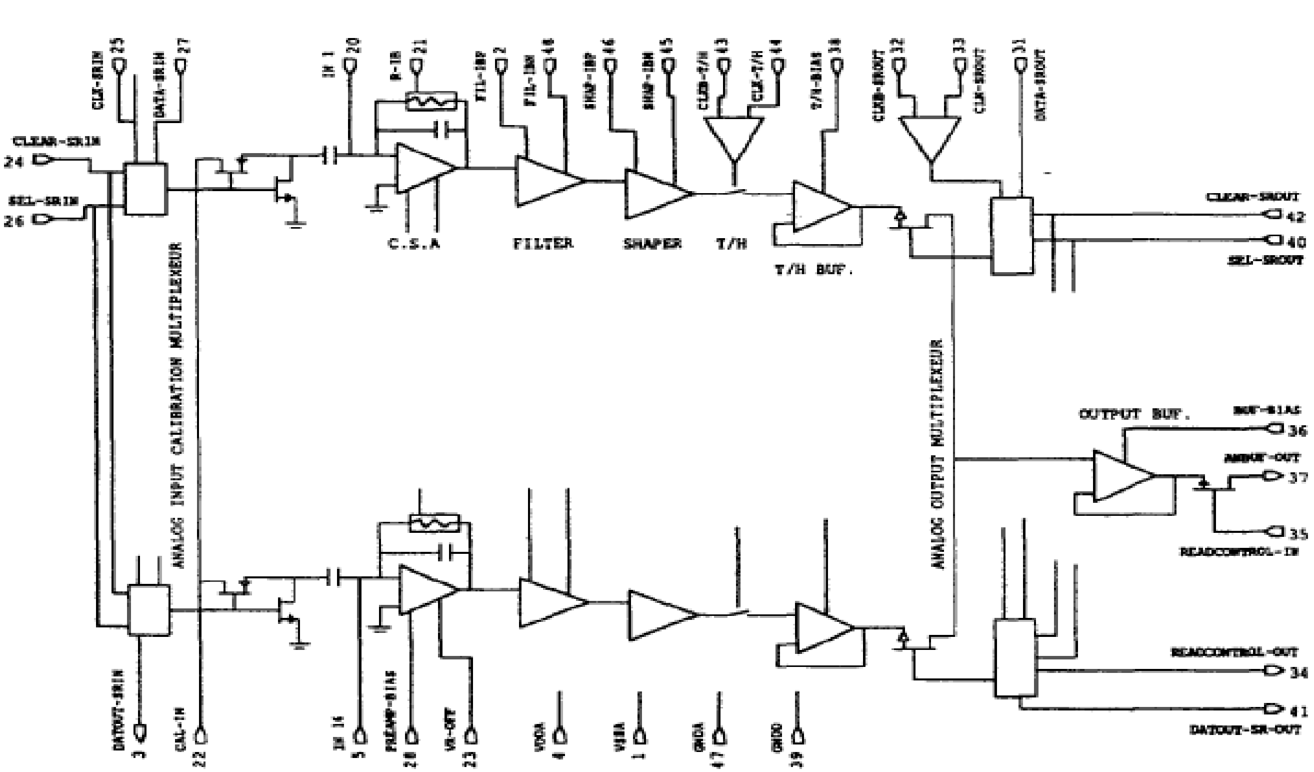
This two terms can be cancelled by simple pole-zero filters

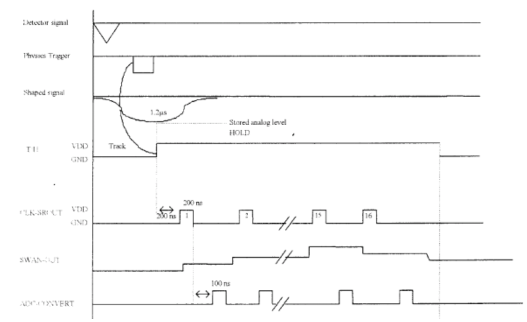
Pole & zero can be determined by calculation anddepends on the geometry, the gas, etc.…

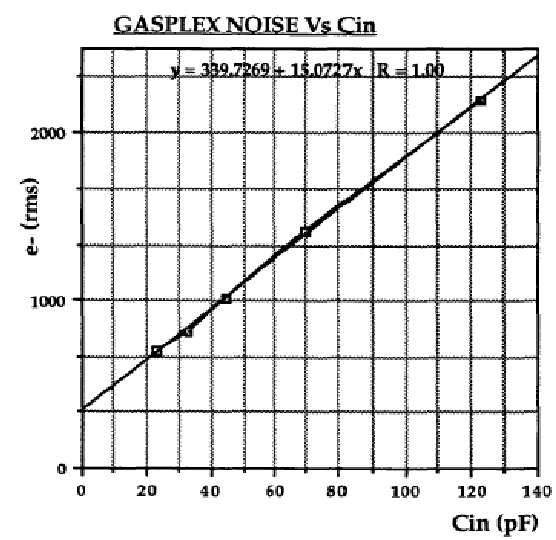


GASS(i)PLEX [SAN 94]

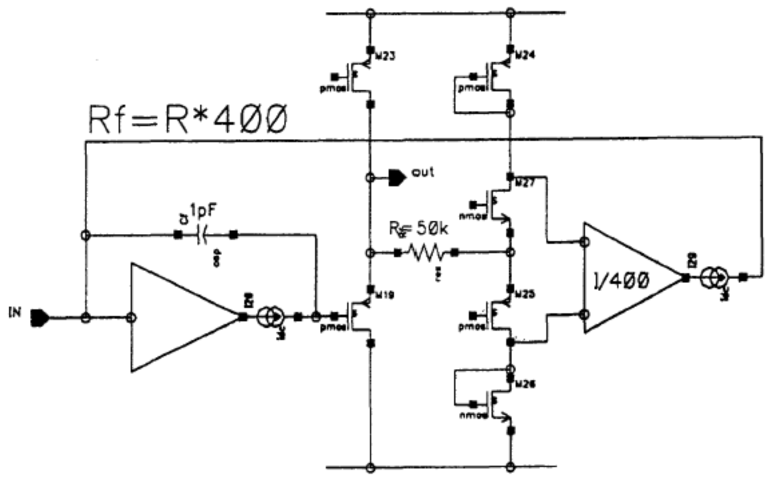
- ✓1.5µm (0.7µM) MIETEC . 16 ch of CSA-SHAPER-T&H
- ✓External TH signal need to be adjusted to catch the peak of the signal
- ✓400ns < Tpeak < 600ns (1.2µm) = maximum latency for TH to be generated
- ✓MULTIPLEXED ANALOG output, AMPLEX like
- ✓10 mW/ Ch.
- ✓Several versions are existing, very popular.
- ✓MANAS= indian version equip 1M Channels of ALICE DiMuon spectrometer



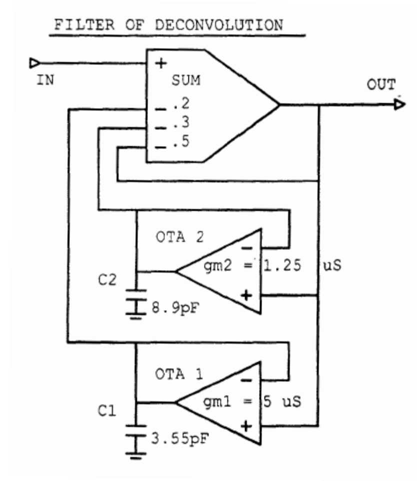




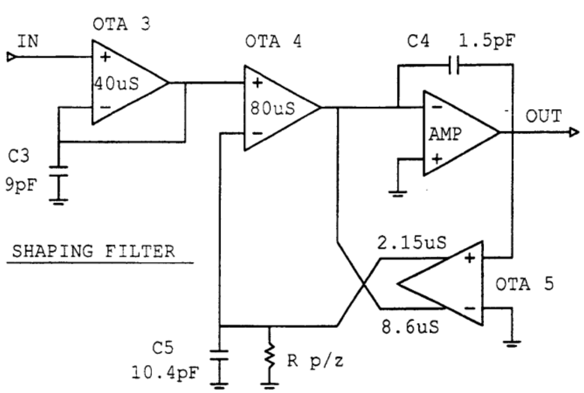
GAS(i)PLEX: several innovations

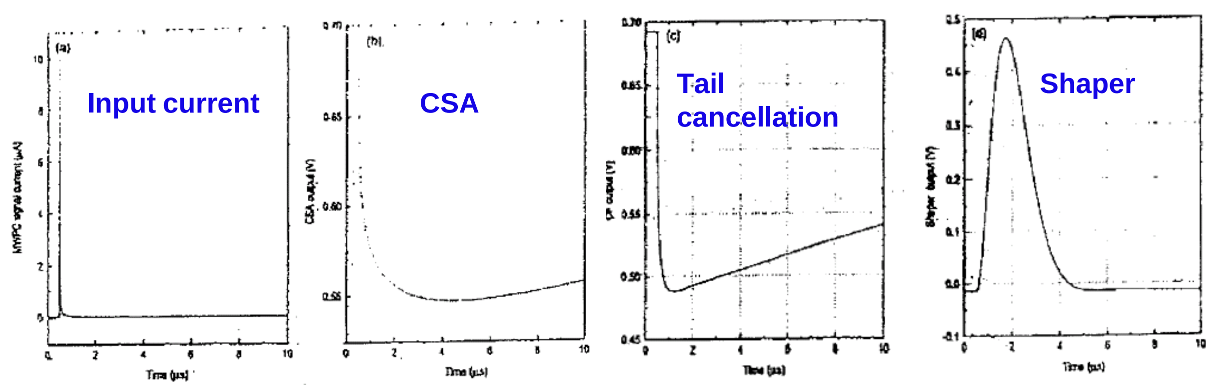


High value of CSA Rf (RFCf= 20μs) made with a resistor + attenuating current conveyor



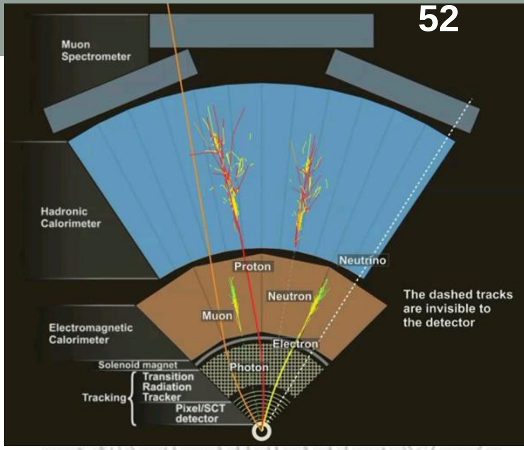
Ion tail cancellation using PZ technique



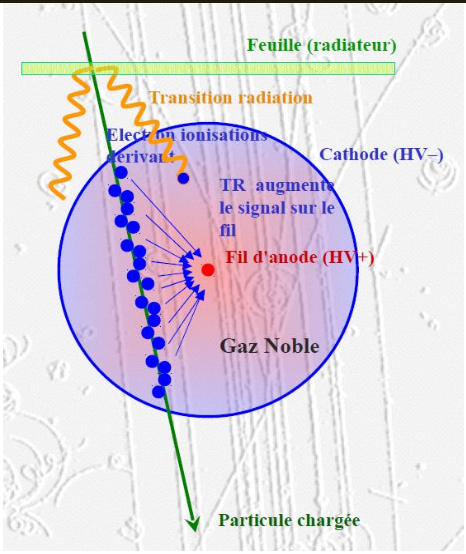


Semi-Gaussian Filter using multiple-loop feedback

Transition Radiation Tracker: un détecteur 2 en 1



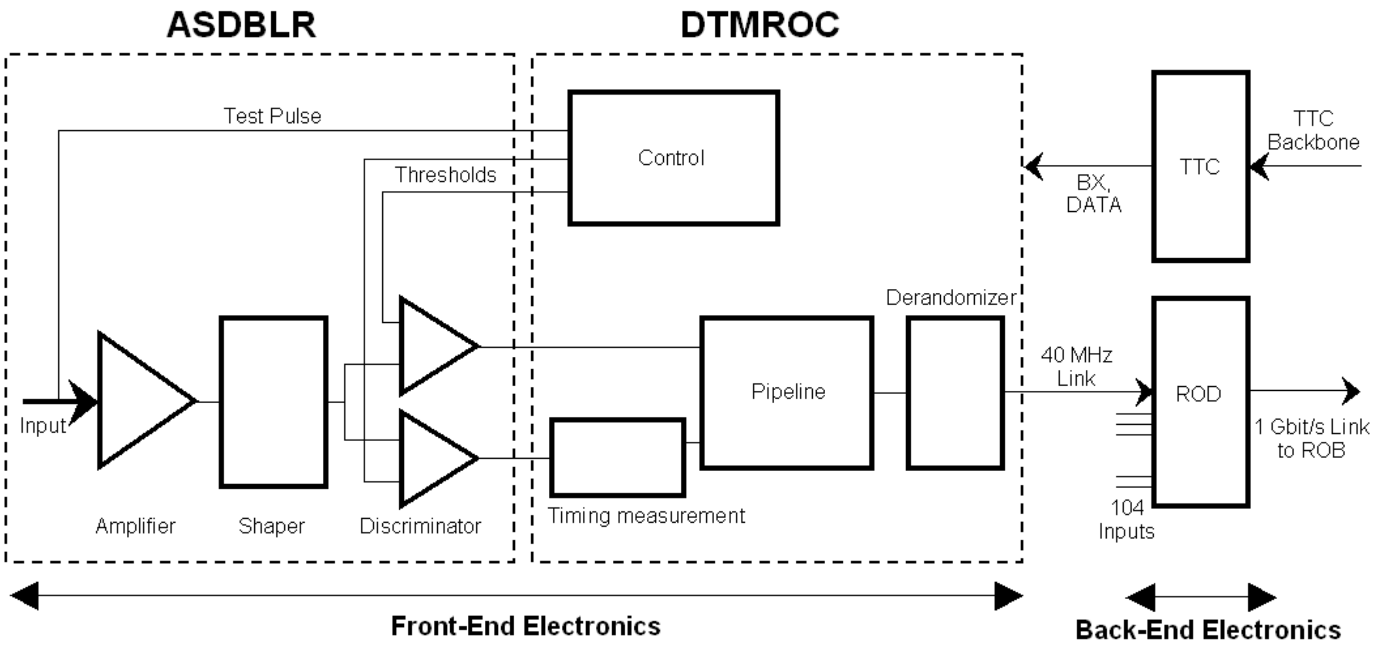
- Trajectographe constitué de pailles (straws)
- Identification de particules grâce au phénomène de radiation de transition dans le radiateur:
  - Electrons => X > 5 keV,
  - 25% de chance de détection/paille,
  - 35 pailles « marquées » par trajectoire

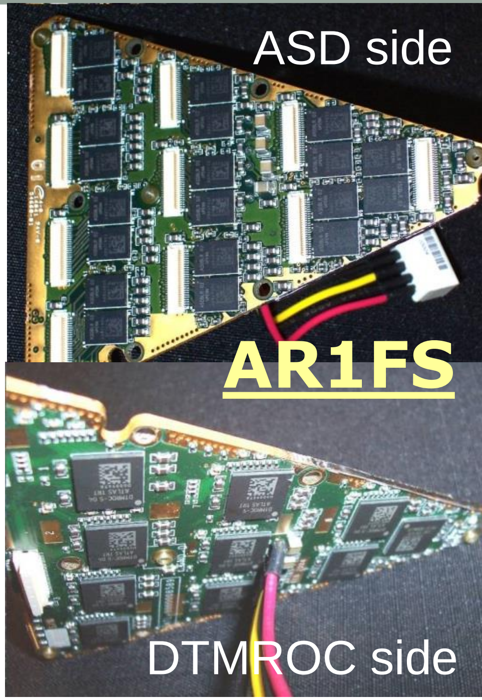


Chambre à dérive longueur (0.37 à 1.44m)

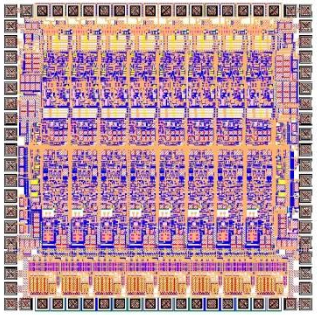
- Fil 31 µm, diamètre paille 4 mm
- V=1530 Volts
- Pression = 1 atm (+10mbar)
- 70% Xe, 27% CO_2, 3% O_2
- Gain : 2.5104
- Position = Temps de dérive
- Temps de dérive max :48 ns
- Résolution spatiale σ~130µm

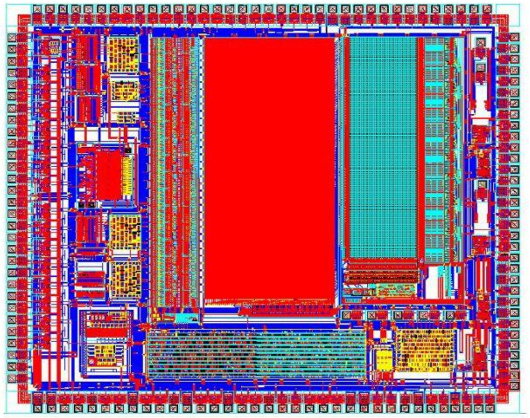
TRT Electronics Overview





- •ASDBLR Die DMILL 0.8µm
- •3.6 x 3.6mm

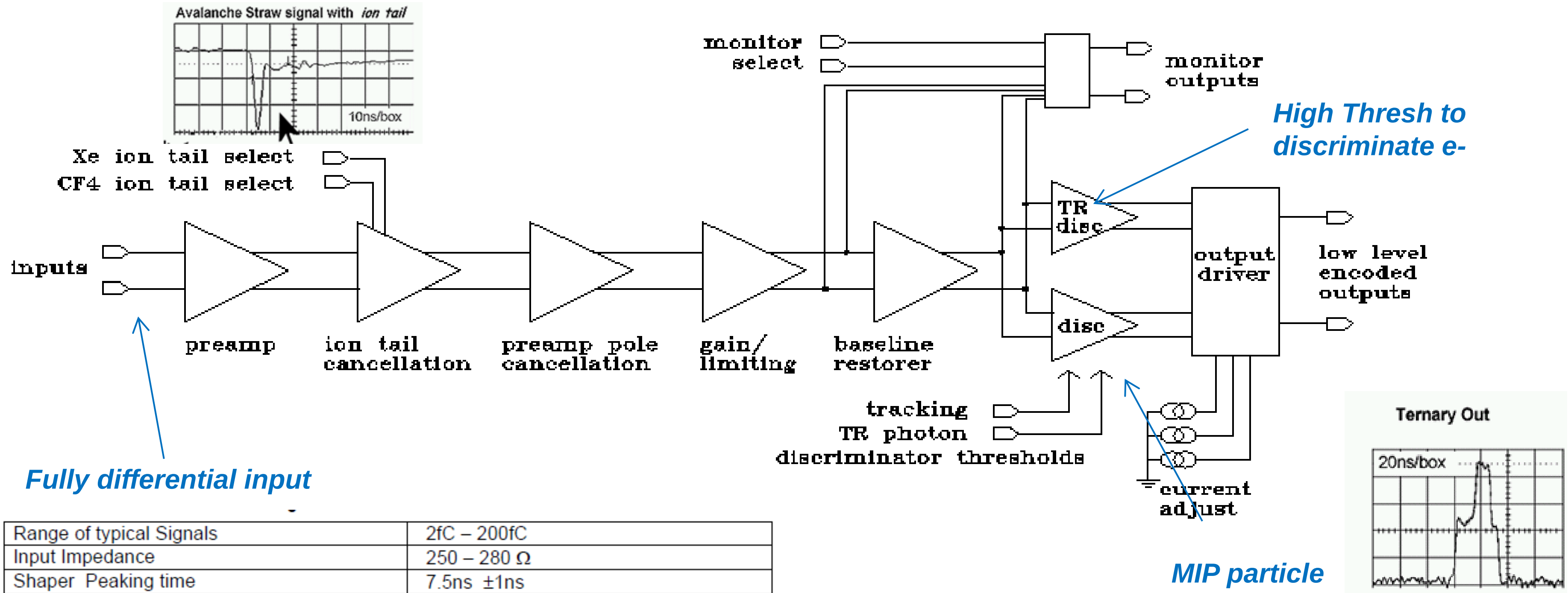




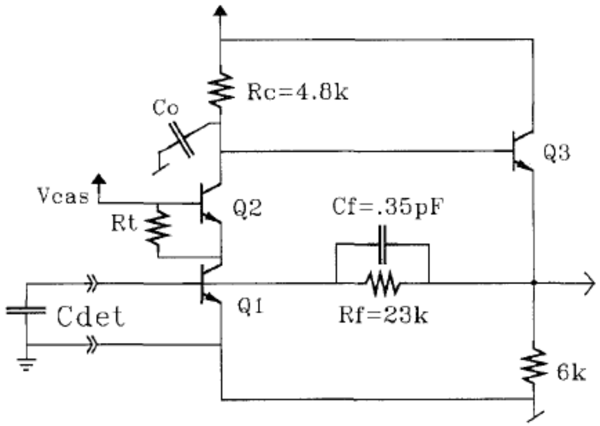
- DTMROC
- IBM 0.25µm
- Size 7.7 x9.3 mm

ASDBLR chip [DRES 01]

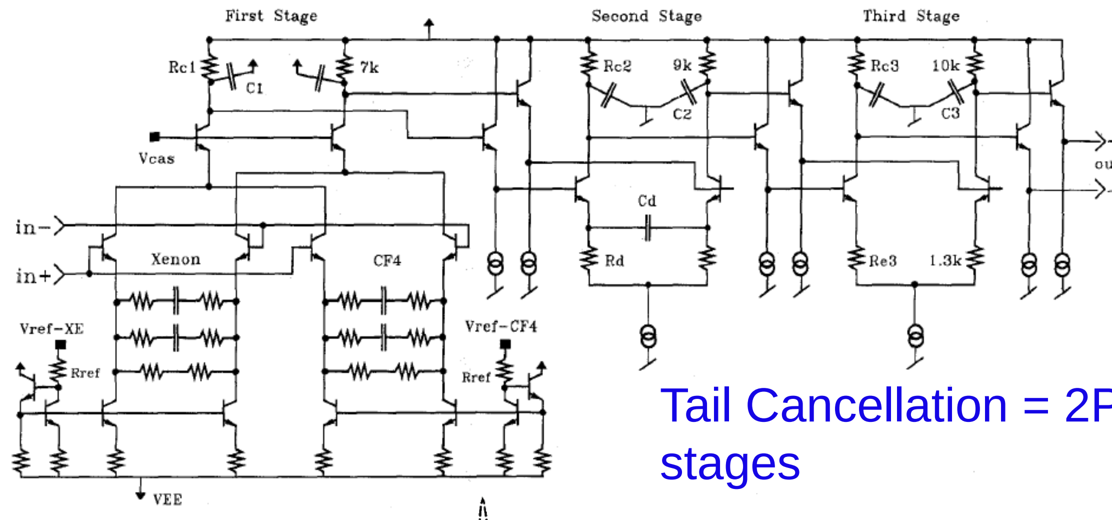
- **ASD chips family (ASD8,…)**
- **DMILL BiCMOS technology**



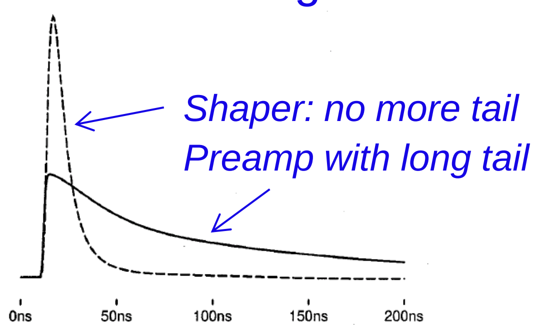
Range of typical Signals	2fC – 200fC
Input Impedance	250 – 280 Ω
Shaper Peaking time	7.5ns ±1ns
Width of Shaped Signal at base	20ns
Maximum Overshoot Area	20%
Low Threshold Range	Noise floor – 10fC
Maximum Trigger Rate	20 MHz
Leading edge time resolution	1ns RMS
Min. Detectable Signal, Low Threshold	2fC (12,500e) in 7.5ns
Low Level Threshold Uniformity	All channels singles rates << 1MHz Ch to Ch deviation < .4fC
Minimum Output Width	5ns
Maximum Discriminator Dead time	5ns
Maximum recovery from 1pC signal	500ns
Peaking time for High Threshold Signal	10ns ± 1.5ns
High Threshold Range	10fC – 120fC
Typical singles trigger rate (Noise)	10 – 50kHz
High Level Threshold Uniformity	< 4fC
Channel to Channel Crosstalk	< 0.5 %
Radiation Hardness (10 year total dose)	1.5Mrad and 1x 10^{14} n/cm^2
Power	< 40mW/ch (< 320mW per chip)



Preamp



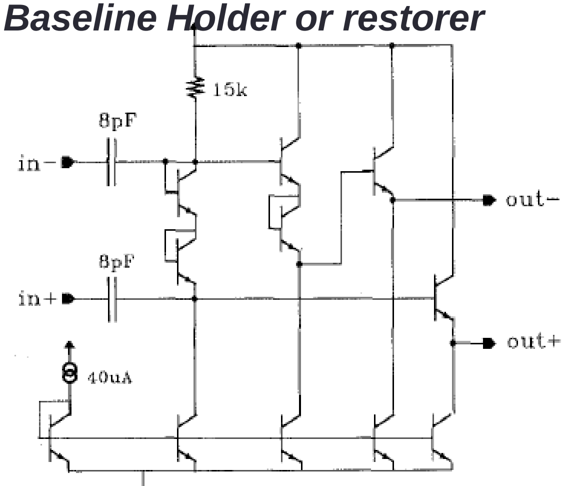
Tail Cancellation = 2PZ stages



AC coupling => zero integral signal

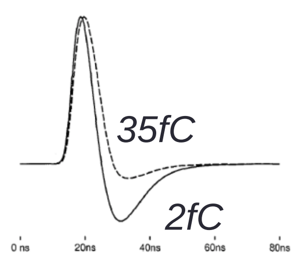
⇒ Negative lobe + high rate=> pileup => baseline shift

⇒ Baseline Holder or restorer



BaseLine Holder

Time cte depend on amplitude



Normalized Shaped signal with BLH => Undershoot decrases for large signals

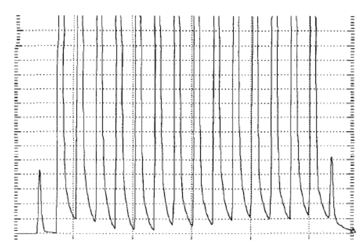


Figure 7: Shaper output (200ns/div). Pileup in a 15 MHz environment of 50fC signals results in an effective threshold shift for two 2fC signals.

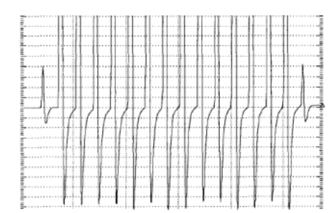
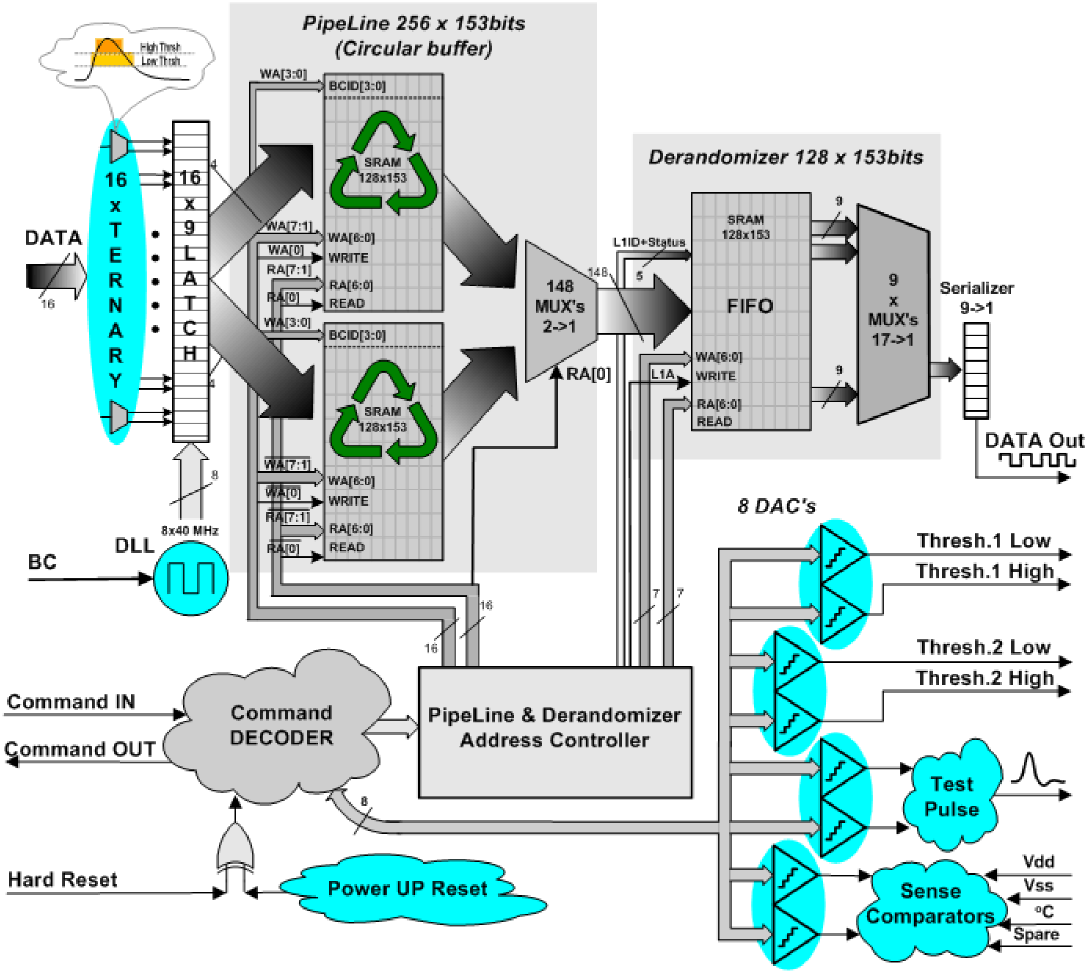
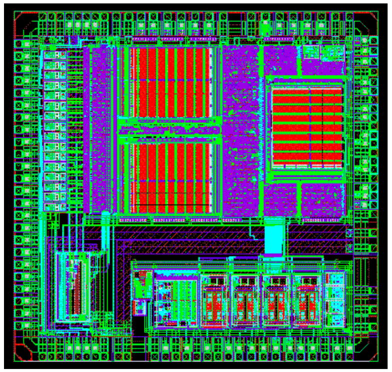


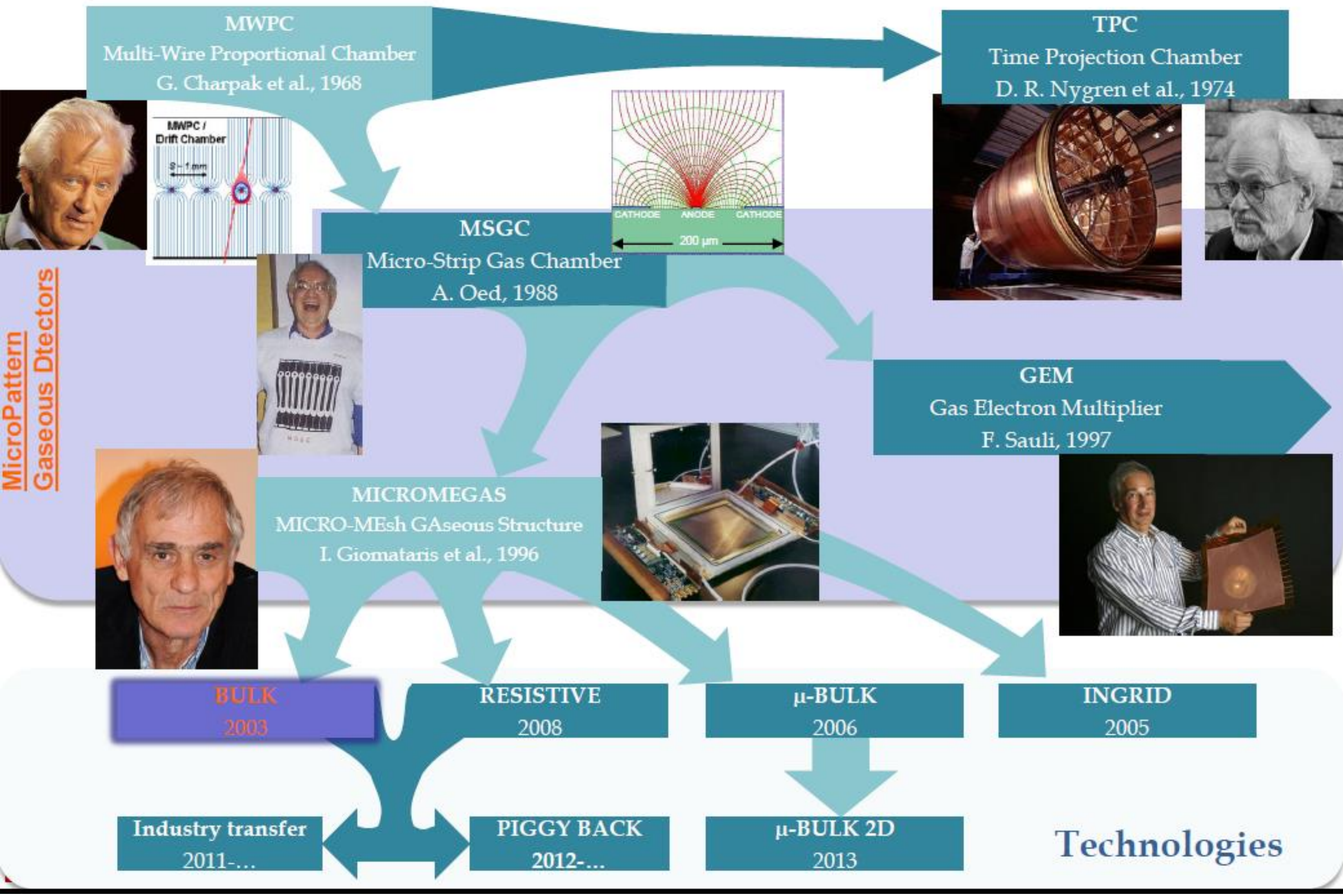
Figure 8: Output of baseline restorer (200ns/div) for the same simulation shown in Figure 7. No voltage shift is observed at the input to the discriminators, where all signals return to baseline within 45ns.

DTMROC chip

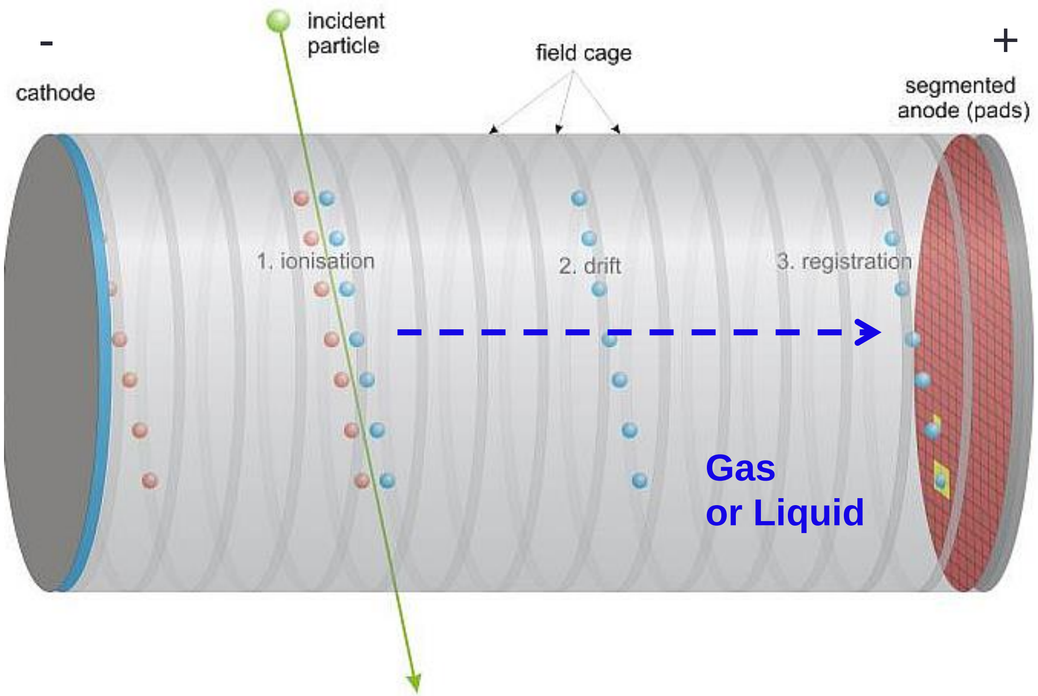




Channels	16
Timing measurements	3 ns binning
Pipeline length	3.2μs (128 LHC bunch Xings)
Bunch-crossing number and event number stored with the data	
Readout of 3 consecutive time-slices on receipt of L1A	
Read-out dead-time	Below 1% at 75kHz L1A rate
Serial data read-out	40Mbit/s
ASDBLR threshold setting	6 bit
Programmable test pulse	1 bit, 2 phases
Power consumption	10mW/channel


MWPC
Multi-Wire Proportional Chamber
G. Charpak et al., 1968
MWPC / Drift Chamber
TPC
Time Projection Chamber
D. R. Nygren et al., 1974
MicroPattern Gaseous Dtectors
CATHODE
ANODE
CATHODE
200 µm
MSGC
Micro-Strip Gas Chamber
A. Oed, 1988
GEM
Gas Electron Multiplier
F. Sauli, 1997
MICROMEGAS
MICRO-MEsh GAseous Structure
I. Giomataris et al., 1996
BULK
2003
RESISTIVE
2008
µ-BULK
2006
INGRID
2005
Industry transfer
2011-…
PIGGY BACK
2012-…
µ-BULK 2D
2013
Technologies

Principle of a TPC



Muliplication readout at anode:

- MWPC (Delphi, ALICE, ALEPH)
- Micromegas (T2K, ILC, ACTAR)
- GEM (ALICE upgrade, ILC)

XY are given by the pad location
Z is given by the time of arrival of drifted e-
dE/dx = charge collected

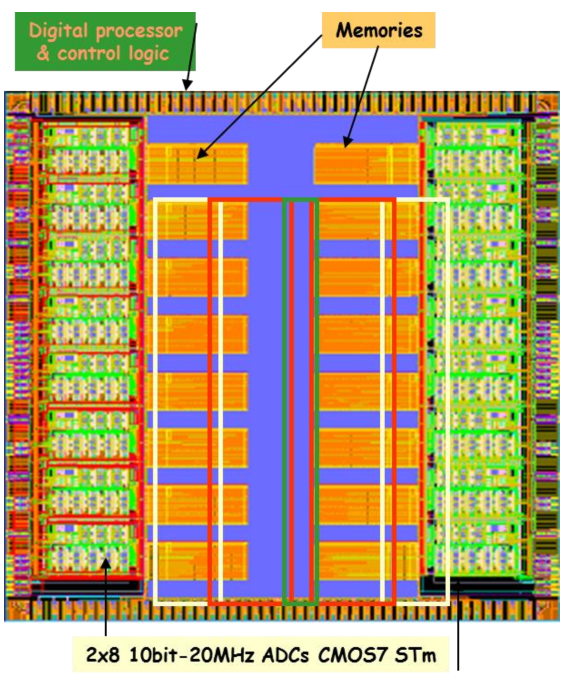
- Very low material budget
- Real 3D trackings
- Complete Tracks and not only points
- Read the complete waveform for each pad, extract time:
  - Analogue memory readout (STAR, T2K)
  - ADC readout (ALICE, STAR …)

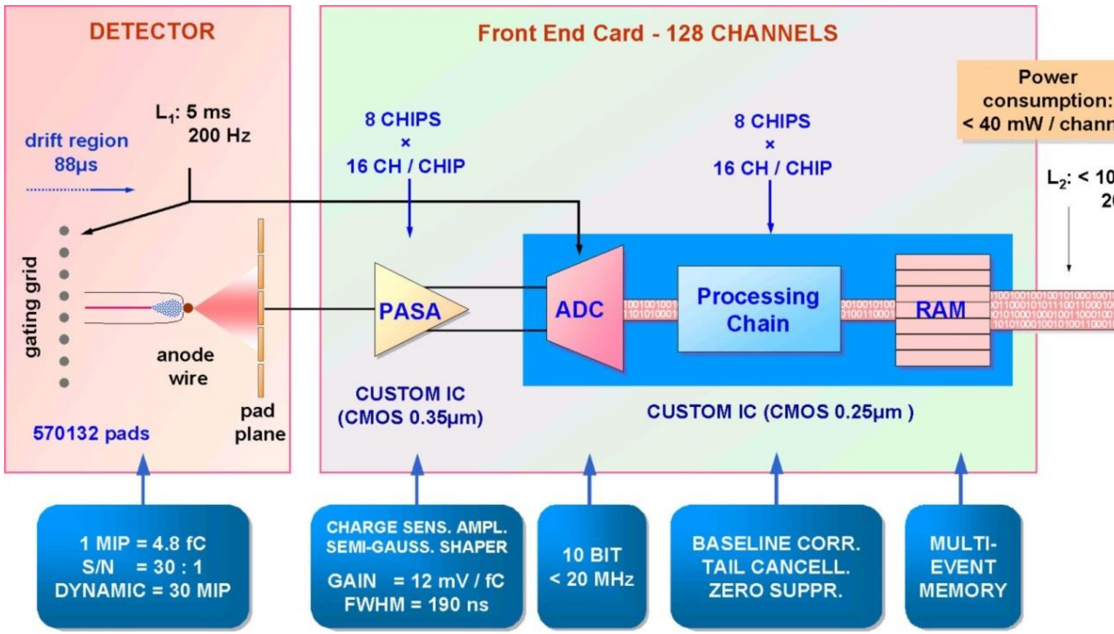
ALTRO for the ALICE TPC [BOE03] [MUS 03]: early digitization

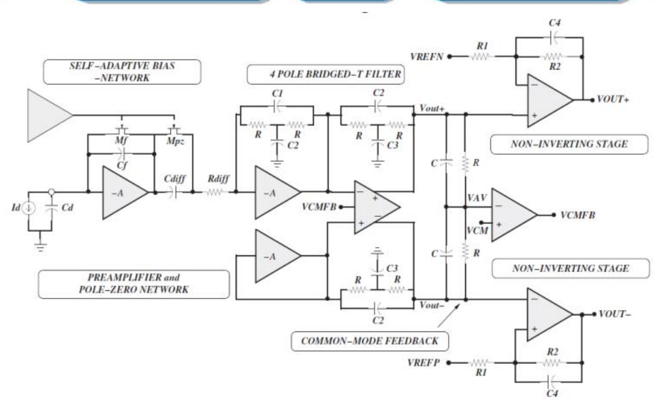
Philosophy: *In (large) detectors, the signals are perturbed by common mode noise, fix pattern parasitics…that makes their discrimination difficult (or zero supress).*
Instead of removing them in the analogue world (grounding…), let us filter them digitally…

- **PASA (AMS 0.35):**
  - 16 CH CSA+ SHAPER
  - AMS 0.35 µm
- **ALTRO (ST 0.25) 64mm²**
  - 16 ADC 10-bit **20**MHz
  - Digital filtering
  - Memories & RO

TOTAL POWER =40 mW/ch







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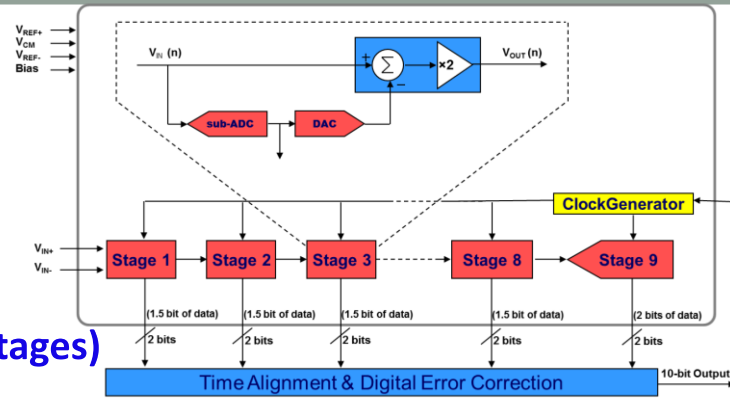
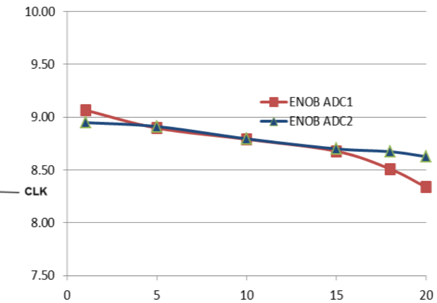
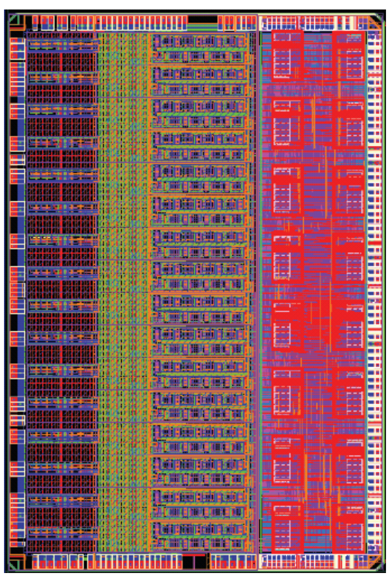
- **ALTRO in a single chip**
  - **Demonstrator for ILC**
  - **16 channels**
  - **CSA+ SHAPER**
  - **40 MHz 10 bit pipeline ADC (1.5bit stages)**
  - **Digital filters**
  - **Readout (40b //bus)**
  - **47 mW, 4.4 mm²/ch**





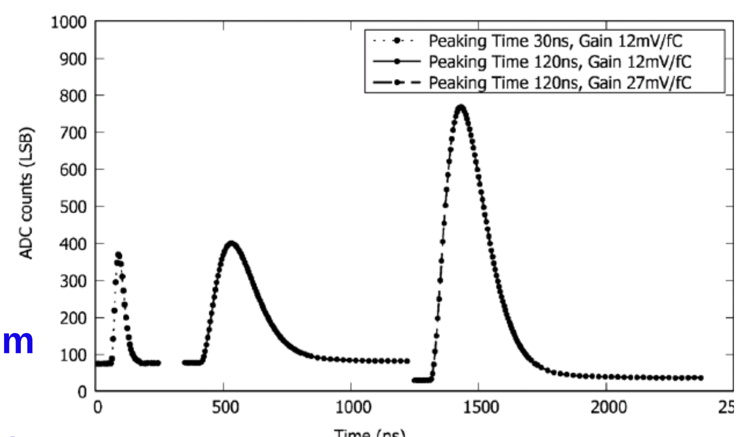
34mW/ch @40MHz
9bit ENOB

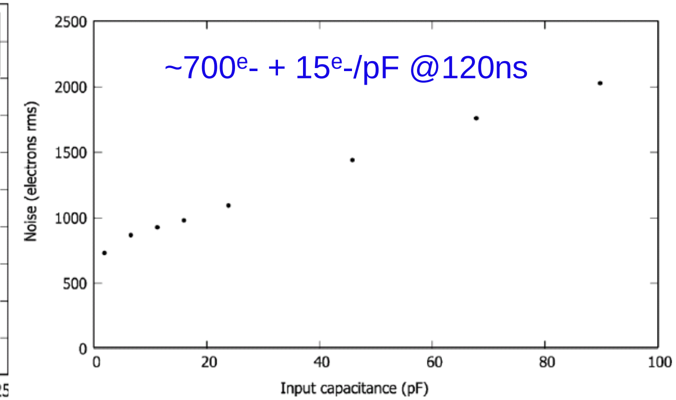
Baseline Correction 1	Removes the systematic offsets that are introduced due to clock noise pickup and switching of the gating grid of the detector. A baseline memory is used for storage of baseline constants which are used for look-up table correction of the base line.
Digital Shaper	Compensates the distortion of the signal shape due to very long ion tails.
Baseline Correction 2	Reduces non-systematic baseline movements based on a moving average filter.
Zero Suppression	Removes samples that fall below a programmable threshold.



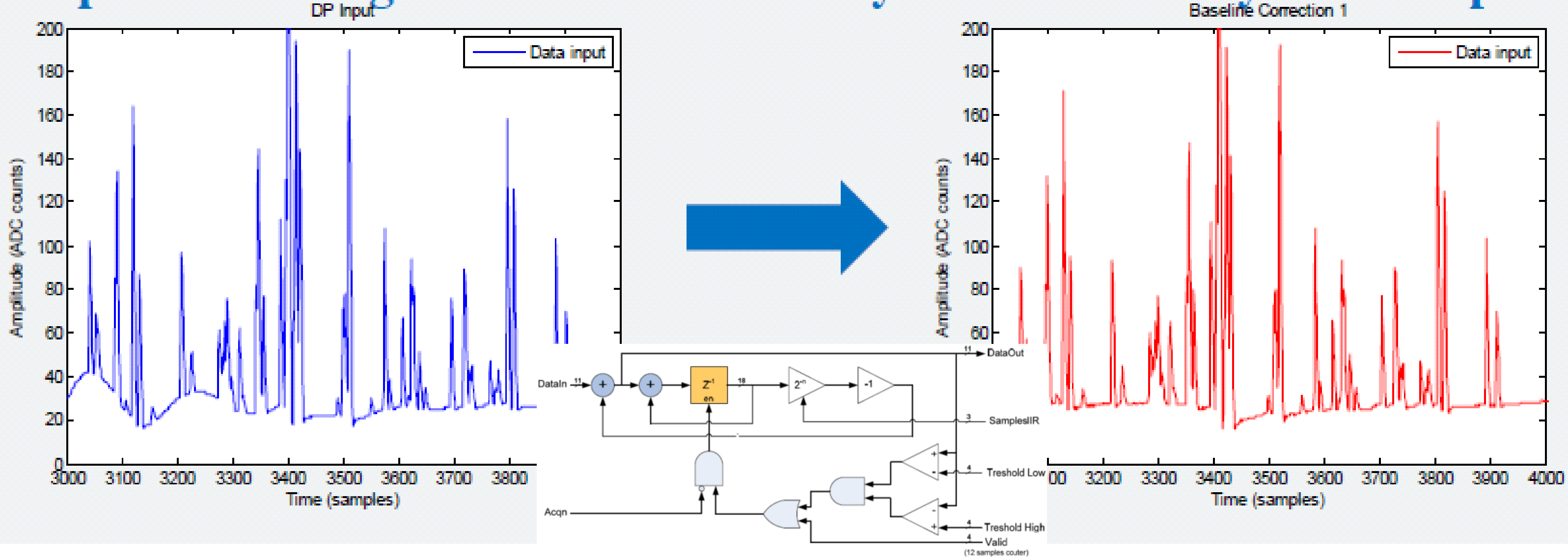
IBM 0.13: 5730µm x 8560µm

1.5nF/ch bypass capacitors
Use of BFMOAT for A/D separation

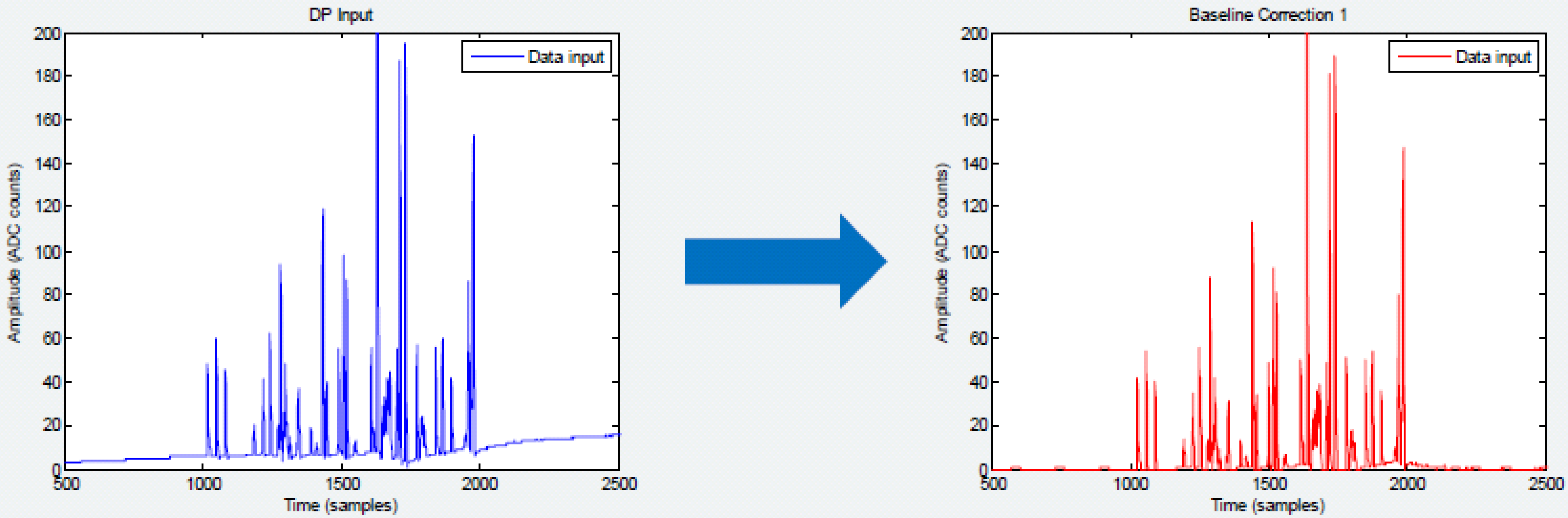




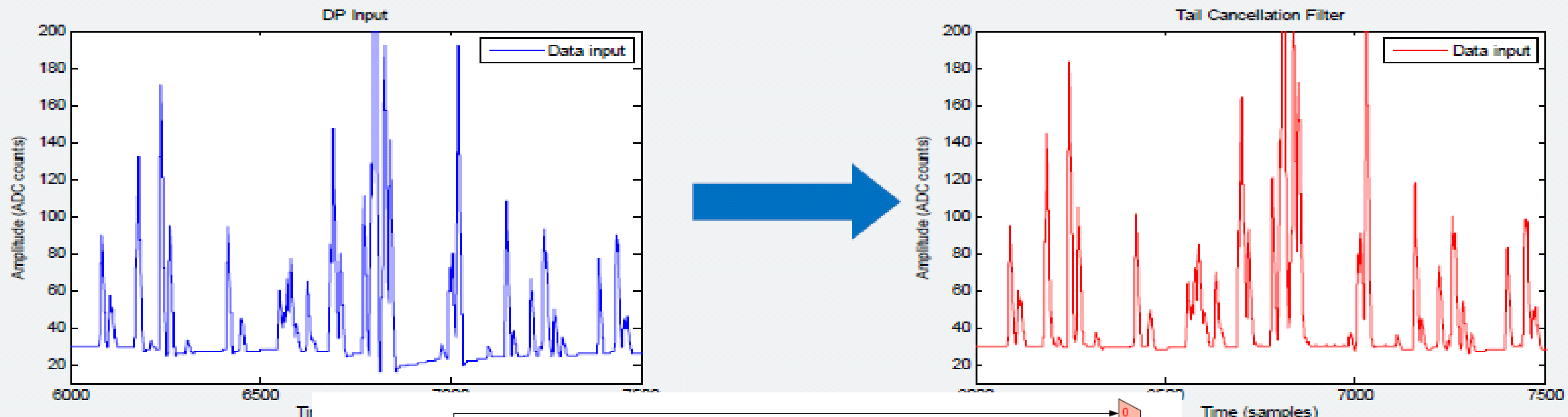
BC1 example test: using the Pedestal Memory to subtract a systematic pattern.

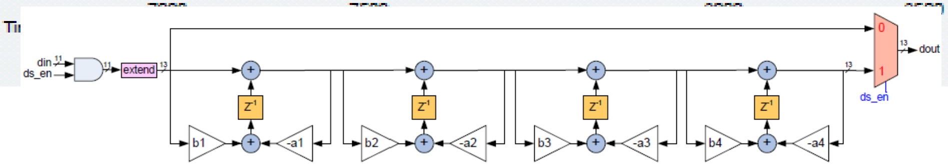


BC1 example test: using the IIR filter to remove slow drifts of the baseline.

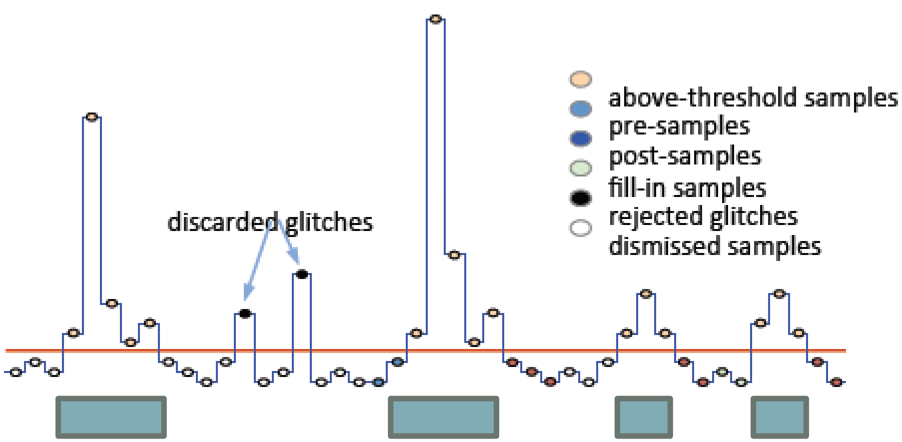


DS example test: removing the undershoot of the analog pulse.

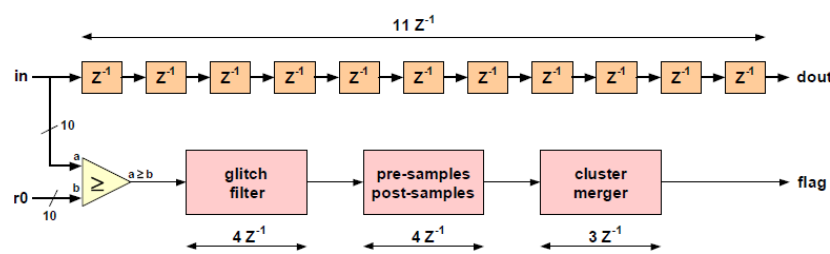




Programmable coeff

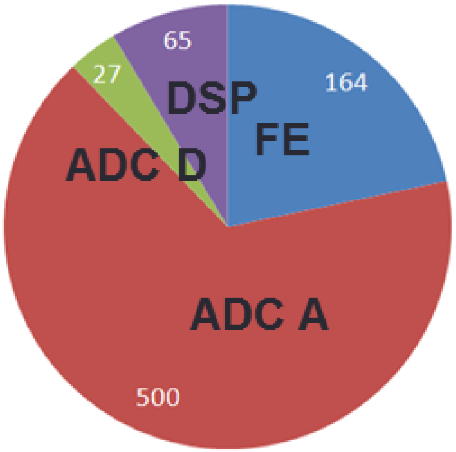


Zero supress

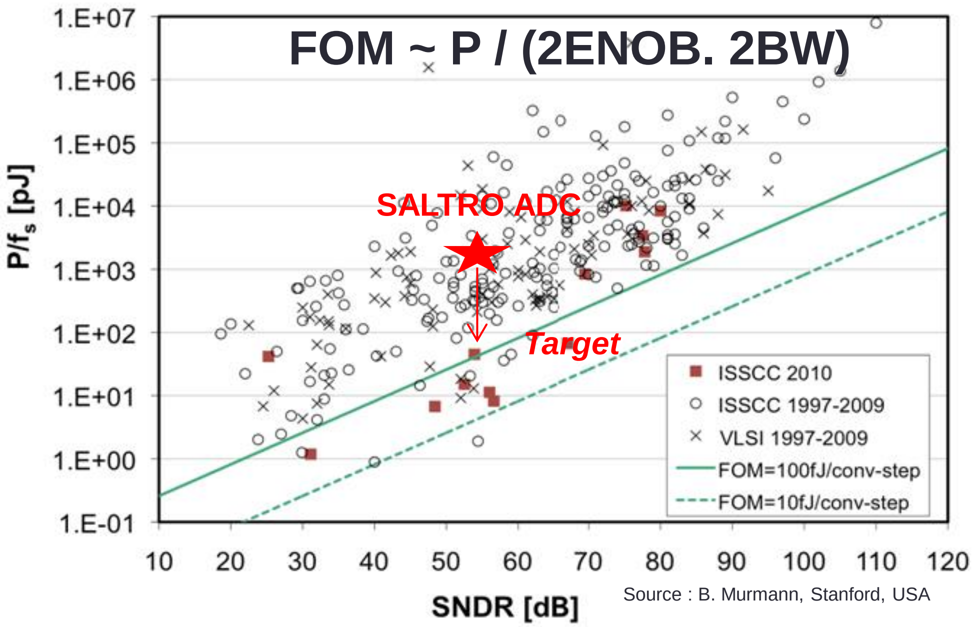


Future of SALTRO-like architecture

- Still too big for high density detectors,
- Too large Power consumption => ADC,
- Large improvements during the last few years (SAR),
- Gain by a factor of 10 seems possible,
- But Power consumption for references or digital corrections are often forgoten in papers,



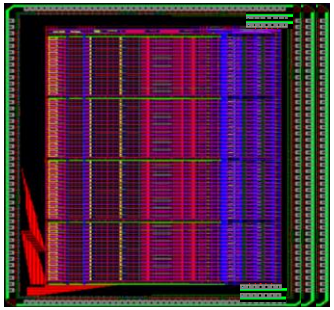
- 2 chips currently under design:
  - GDSP (CMS Muon + ILC)
    - IBM 0.13, 128 ch
  - SAMPA (ALiCE TPC + DIMuon)
    TSMC01.3, 32 ch



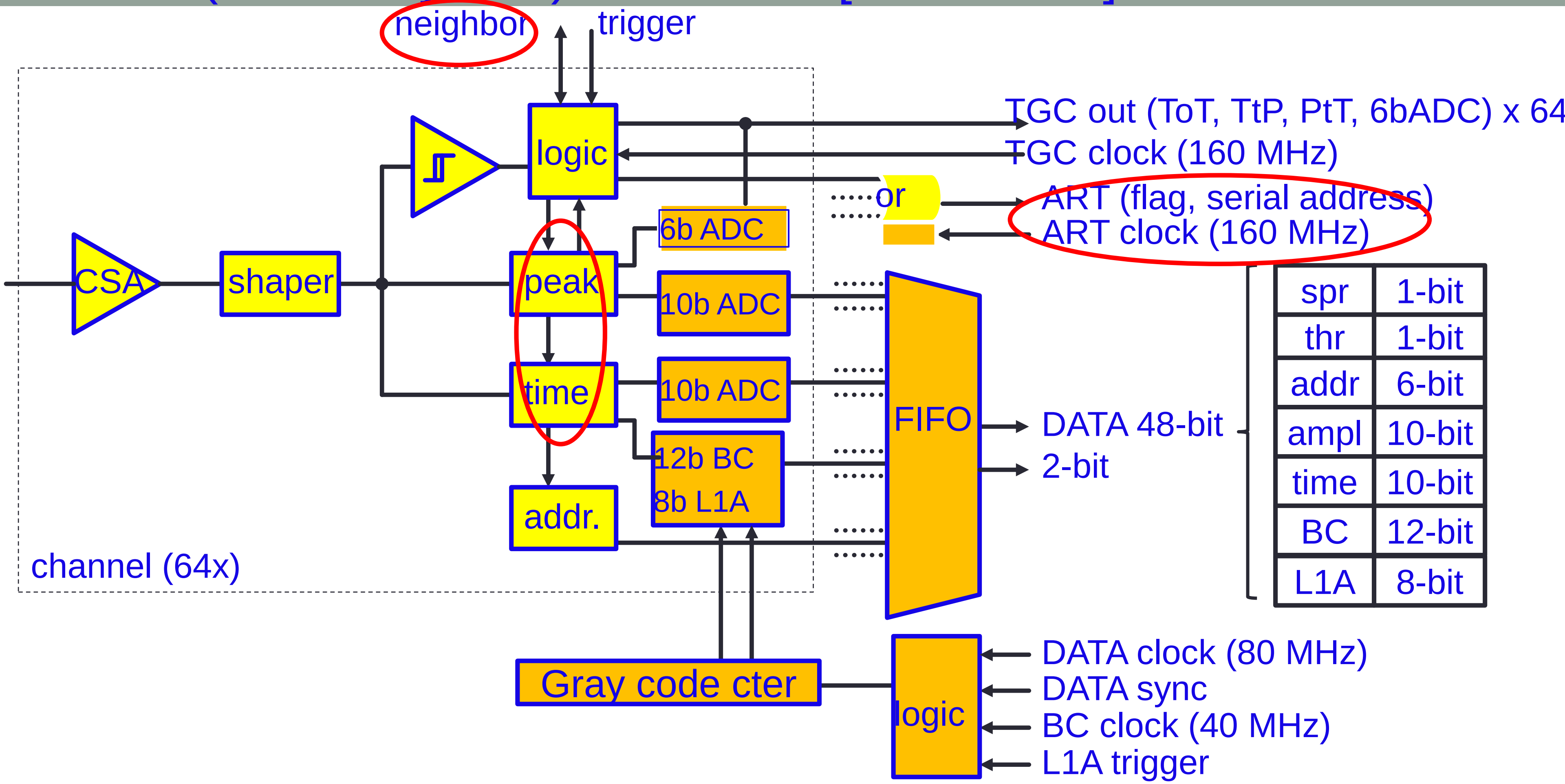
Source : B. Murmann, Stanford, USA

- New electronics for HL-LHC Muon chambers (>1000 m^2)
- ITGC and resistive Micromegas
- Now same detectors for the trigger and and the tracking.
  - ⇒25ns Real time position of the hits:
  - ⇒Fast shaping required
  - ⇒Fine measurements :
    - ⇒Timing used for track angle measurement (mini TPC mode).
    - ⇒« risetime measurement »
    - ⇒High dynamic range (gas)
    - ⇒Good resolution required => centroïd for position.

Expected size =9x9 mm



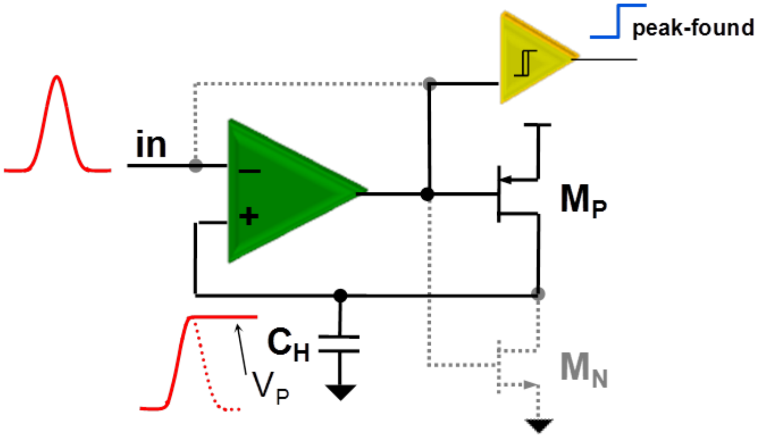
- Totally Asynchronous architecture:
  - Discri + Peak detectors
- Treatment on hit channels + neighbours
- On chip digitization.
- Ultra versatile: 10pF-200pF, 25ns-200ns, all polarities
- 64 channels; IBM 0.13
- 4mW/Ch
- VMM1 tested succesfully, VMM2 is comming soon

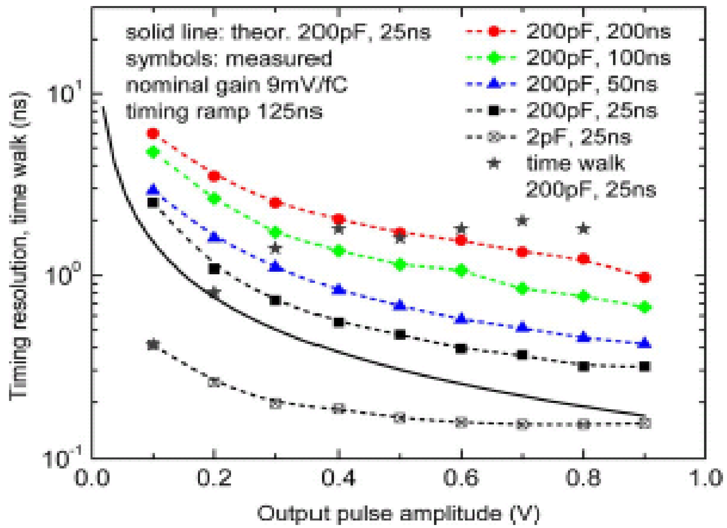


- TGC: 64 outputs, PtT, 6-bit ADC 25ns serial with dedicated clock
- ART: flag and address serialized with dedicated clock
- 10-bit ADCs 200ns for amplitude and timing, digital memories
- Gray-code counters for BC-ID (12-bit) and L1A-ID (8-bit)
- 2-bit DATA output with dedicated sync and 80 MHz clock

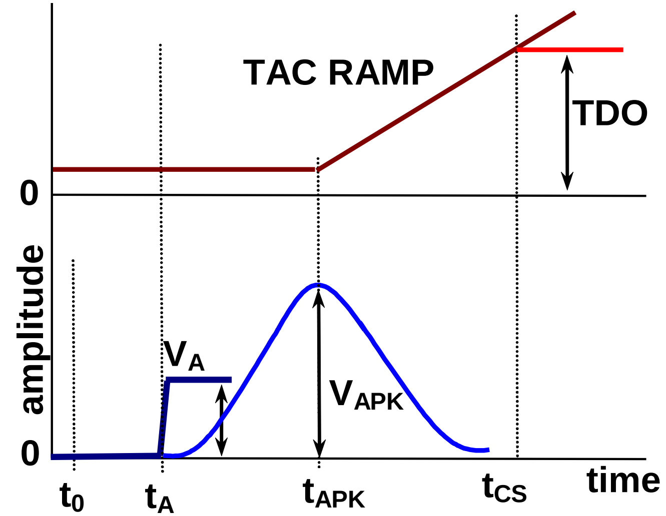
VMM timing

- Timing achieved by:
  - peak detection together with amplitude
  - enabled by discri
  - ramp TAC
- Less sensitive to common mode noise an time walk
- Pulse risetime used as delay, allowing measurement of neighbors under threshold



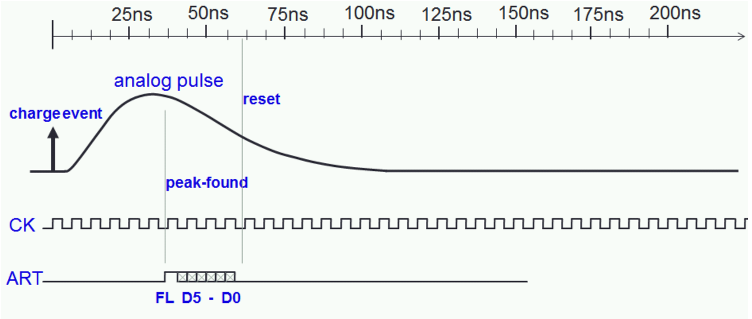


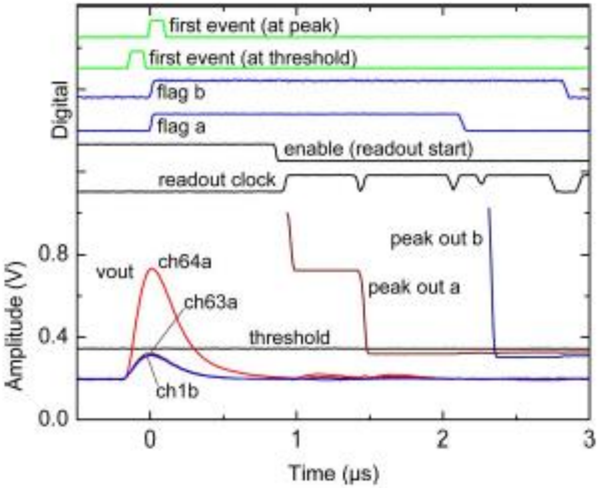
Sub ns timing resolution



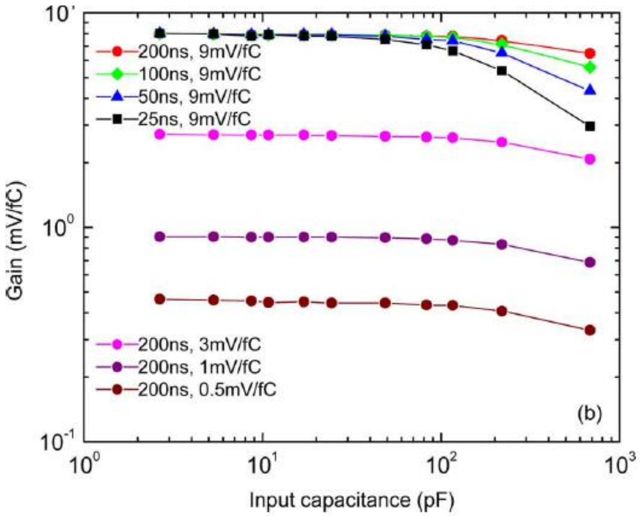
VMM chips

Real Time Address of first event transmission (160 MHz clock)

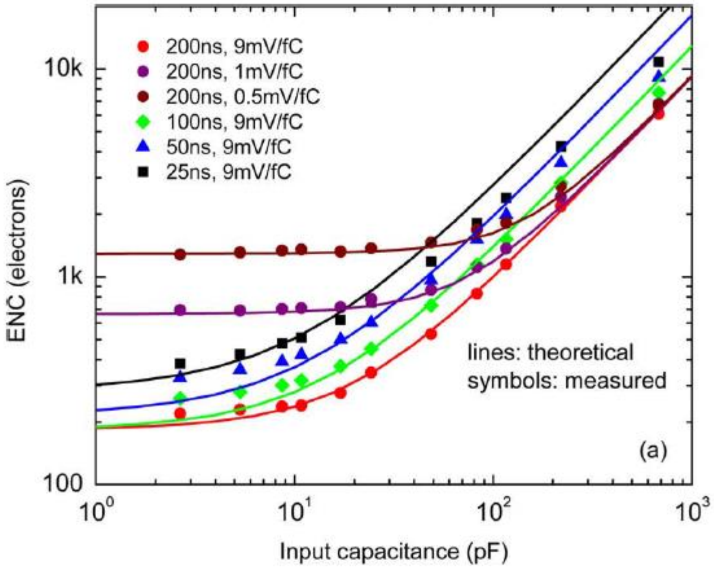




Neighbour channel processing:First event detected by channel Xing Enables peak detectors of the channel + Neighbours + readout



Gain independant of Cd on a very large range



Extremely good ENC (for low and high values of C_D)

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